Version	Date/ Datum	Initiated by/ Veranlasser	Reason of modification / Grund der Änderung item, section / Position, Absatz
A	12/1/2005	HB Lim	ECN# SJ5-1079 New Spec
B	Feb 27th, 2006	Lim Hooi Bin	TAB connection pin out changed on D0 Modified Product drawing to add Polarizer and IC dimensions Module thickness changed from 1.70 +/- 0.1 mm to 1.80 +/- 0.10 mm Added DC operating temperature range of -30 °C to +70 °C Added of handling and ESD procedure Included operating lifetime of 3.5k @ 25°C on White and Ocean Blue products

The document No.
Die Unterlage mit der Nr.:

A63857-H36XX-D000-0B-7680

Issue:
Version:

00;00

is no longer valid and must be discarded

Applicable Area - Scope / Gültigkeitsbereich	
Corporation:	OSRAM Opto Semiconductors
Location:	<location>
Cluster:	<cluster>
Unit:	<Unit>
SubUnit:	<SubUnit>
Process:	<process>

Revision Log

Rev.	Description	Orig. By	ECN # / Date
A	New Spec	Lim Hooi Bin	ECN# SJ5-1079/ 1st Dec 2005
B	TAB connection pin out changed on D0 Modified Product drawing to add Polarizer and IC dimensions Module thickness changed from 1.70 +/- 0.1 mm to 1.80 +/- 0.10 mm Added DC operating temperature range of -30 ^{o}C to +70 ^{o}C Added of handling and ESD procedure Included operating lifetime of 3.5k @ 25^{o}C on White and Ocean Blue products	Lim Hooi Bin	

CONTENT Page

1. TITLE

1.1 Product Specification for Pictiva™ 96X16 OLED Module, SSD0303, Hilo 1-bit H36XX-OS096016PP08MXXB10

2. PURPOSE

2.1. This product specification is specifically for OLED Hilo Module H36XX.

3. SCOPE

3.1 This product specification is applicable to all H36XX modules.

4. REFERENCE DOCUMENTS

4.1 C63062-H36XX-A001-*	Hilo Module Product Drawing (with TAB IC)SSD0303 Solomon Systech SSD0303 96X64, Dot Matrix OLED/PLED Segment/Common Driver with Controller Remarks : The difference between SSD1303 and 0303 is that SSD0303 has the I^2C interface feature whereas the SSD1303 only carries serial and parallel interface

5. OTHER REQUIREMENTS

5.1 FEATURES, FUNCTIONS, and REQUIREMENTS

5.1.1 Product Summary:

General OLED Module Description

Display Format	96 columns x 16 rows
Pixel Pitch	0.22 (W) x 0.22 (H) mm
Pixel Size	0.19 (W) x 0.19 (H) mm
Display Diagonal	0.8”
Color	Monochrome
Grayscale	1 bit
Active Area	20.90 (W) X 3.44 (H) mm
Viewing Area	22.90 (W) X 5.44 (H) mm
Module Size	26.83 (W) X 24.80 (H) X 1.8 (T) mm (TAB is foldable)
Glass Size	26.83 (W) X 10.30 (H) X 1.8 (T) mm (including polarizer)
Driver IC	SSD0303
Packaging and Interconnect	TAB (TCP)
Bezel	None
OLED Power Supply	User Configurable Single or Dual voltage supplies

5.1.2 Part Number:

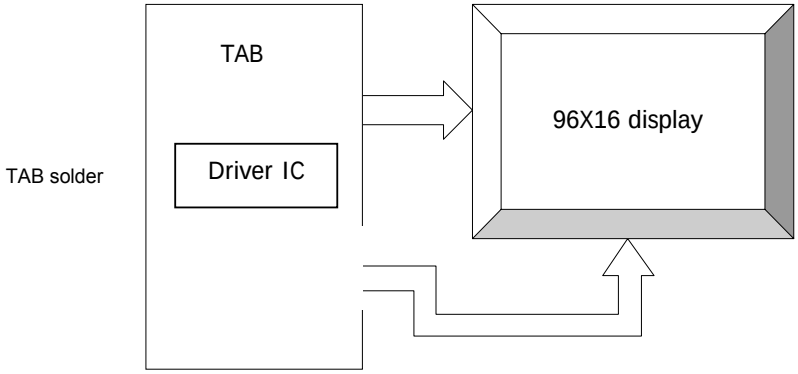
Part Number Description

Part Number	Color	Factory Code
OS096016PP08MW1B10	Galaxy White	H3600
OS096016PP08MB2B10	Ocean Blue	H3610
OS096016PP08MY0B10	Elegance Yellow	H3650
OS096016PP08MG1B10	Lime Green	H3665
OS096016PP08MO1B10	Tiger Orange	H3675
OS096016PP08MO2B10	Golden Orange	H3672*

Remarks: H3672-OS096016PP08MO2B10 (Golden Orange) is an optional color, check with OSRAM for availability.

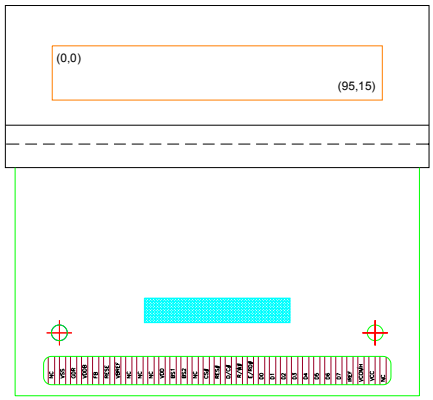
5.1.3 Electrical Characteristics

Functional Block Diagram:



Overall block diagram of display module assembly and interface

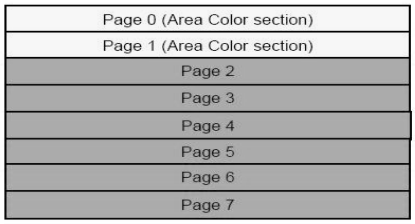
5.1.4 Graphic Area Pixel Mapping:



Pixel mapping

5.1.5 Graphic Display Data RAM (GDDRAM) access

To access display data RAM, the D/C pin should be pulled high. In SSD1303/SSD0303, the RAM is divided into eight pages, from page 0 to page 7, as shown in below Figure.



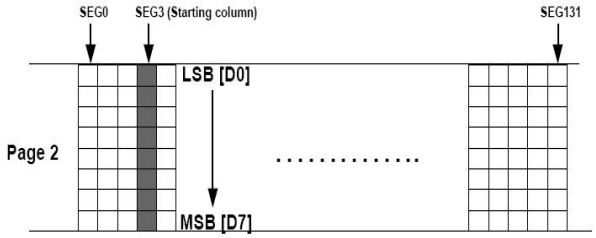
GDDRAM pages structure in SSD1303/SSD0303

In GDDRAM, page 0 and 1 are belonged to area color section with resolution 132x16. Page 2 to 7 is used for monochrome 132x48 dot matrix display.

In normal display data RAM read or write mode, the following steps are required to define the starting RAM access pointer location:

- Set the page address of the target display location by command B0h to B7h.
- Set the lower column address of pointer by command 00h~0Fh.
- Set the upper column address of pointer by command 10h~1Fh.

Let's take an example. Now page address is set to B2h, lower column address is 03h and upper column address is 00h. The RAM access pointer is located as shown in below Figure. The input data byte will be written into RAM position of column 3.



Example of GDDRAM access location setting

5.1.6 Duty Cycle:

The pixel rows are multiplexed and will operate at a nominal duty cycle of 1/16. The default duty cycle is 1/64. During initialization a software command must be used to set the required duty cycle.

5.1.7 Interface Pin Out:

TAB Connection Pin Out

PIN	Name	DESCRIPTION				
1	NC	No connect.				
2	VSS	Ground.				
3	GDR	Gate Drive for Multiplier. This output pin drives the gate of the external NMOS of the booster circuit.				
4	VDDB	Power supply pin for the GDR pin buffer.				
5	FB	Feedback Resistor input for Multiplier				
6	RESE	This pin connects to the source current pin of the external NMOS of the booster circuit.				
7	VBREF	Voltage Reference for Multiplier				
8	NC	No connect.				
9	NC	No connect.				
10	NC	No connect.				
11	VDD	Positive logic supply voltage.				
12	BS1	Interface Selection Pin 1: See BS2 below				
13	BS2	Interface Selection Pin 2:				
			6800 Parallel	8080 Parallel	Serial	I^2C
		BS1	0	1	0	1
		BS2	1	1	0	0
14	NC (CL)	Clock Input. Not used (must be NC)				
15	CS#	Chip Select				
16	RES#	Reset				
17	D/C	HIGH = Bus contains data for DDRAM, LOW = Bus contains command.				
18	R/W (WR#)	Read/Write selector for 68 series; Write strobe for 80 series				
19	E (RD#)	E clock for 68 series; RD strobe for 80 series				
		Parallel		Serial	I^2C	
20	D0	Parallel Data 0		Serial Clock	Serial Clock	
21	D1	Parallel Data 1		Data	Serial Data Input	
22	D2	Parallel Data 2		Floating	Serial Data Output	
23	D3	Parallel Data 3		NC	NC	
24	D4	Parallel Data 4		NC	NC	
25	D5	Parallel Data 5		NC	NC	
26	D6	Parallel Data 6		NC	NC	
27	D7	Parallel Data 7		NC	NC	
28	IREF	Segment (Column) Current Reference. A resistor should be connected between this pin and VSS.				
29	VCOMH	Common (Row) High Voltage, a capacitor should be connected between this pin and VSS				
30	VCC(VLL)	OLED power supply voltage VCC (VLL)				
31	NC	No connect.				

5.1.8 Absolute Maximum Ratings:

Absolute Maximum Ratings

Symbol	Description	Range	Unit
VDD	Supply Voltage for logic	-0.3 to +4.0	V
VCC	Supply Voltage for driver	0 to +16	V
Vin	Input Voltage	VSS-0.3 to VDD+0.4	V
Top	Operating Temperature	-30 to +70	ºC
Tstg	Storage Temperature	-40 to +70	ºC

5.1.9 DC Characteristics of Complete Module:

(-30°C to +70°C Temperature Range, except as noted)

Recommended DC Operating Conditions

Description		Symbol	Min.	Typ.	Max.	Unit
Logic operating voltage		VDD	2.4	3.0	3.5	V
OLED driver input voltage		VCC	8.0	9.0	10.0	V
VDD Operating Current		IDD	-	-	650	μA
VCC Operating Current		ICC	See Table below			
Driver Sleep Mode Current (at 25°C)		ISL	-	-	5.0	μA
Logic input voltage	High	VIH	.8 *VDD	-	VDD	V
	Low	VIL	0	-	.2*VDD	V
Logic output voltage	High (IOH=-.5mA)	VOH	.9 *VDD	-	VDD	V
	Low (IOL=.5mA)	VOL	0	-	.1*VDD	V

ICC Operating Current (VCC, All pixels ON, Luminance at typical value)

Color	Symbol	Min.	Typ.	Max.	Unit
Galaxy White/ Ocean Blue	ICC	4.0	4.5	5.0	mA
Elegance Yellow	ICC	2.0	2.5	3.0	mA
Elegance Yellow (High Luminance) / Lime Green / Tiger Orange/ Golden Orange	ICC	3.5	4.0	4.5	mA

5.1.10 Power Consumption:

(VDD= 3.0V, VCC = 9V, Frame Frequency = 150 Hz, unless otherwise stated)

Power Consumption (External Vcc mode)

		Typical Power Consumption* (mW), Dual supply (VDD, VCC)				
Color	**Typical Luminance** cd/m²	Power Save mode (Sleep mode)	All pixels ON @ typical brightness	10% ON @ typical brightness	10% ON @ 15% of typical	5% ON @ 15% of typical
Galaxy White	80	0.012	40	7	3	2
Ocean Blue	30	0.012	40	7	3	2
Elegance Yellow	100	0.012	22	5	2	2
Elegance Yellow (High Luminance)	200	0.012	38	7	2.5	2.5
Lime Green	120	0.012	38	7	2.5	2.5
Tiger Orange	50	0.012	38	7	2.5	2.5
Golden Orange	60	0.012	38	7	2.5	2.5

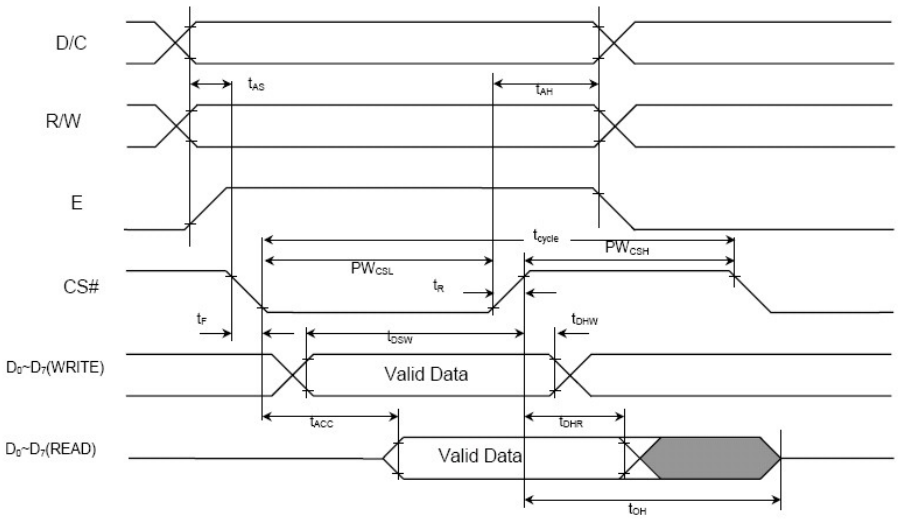
Note: For Single Supply configuration (VDD only), allow 20% higher power consumption for efficiency loss of the optional DC-DC converter.

5.1.11 AC Timing Characteristics:

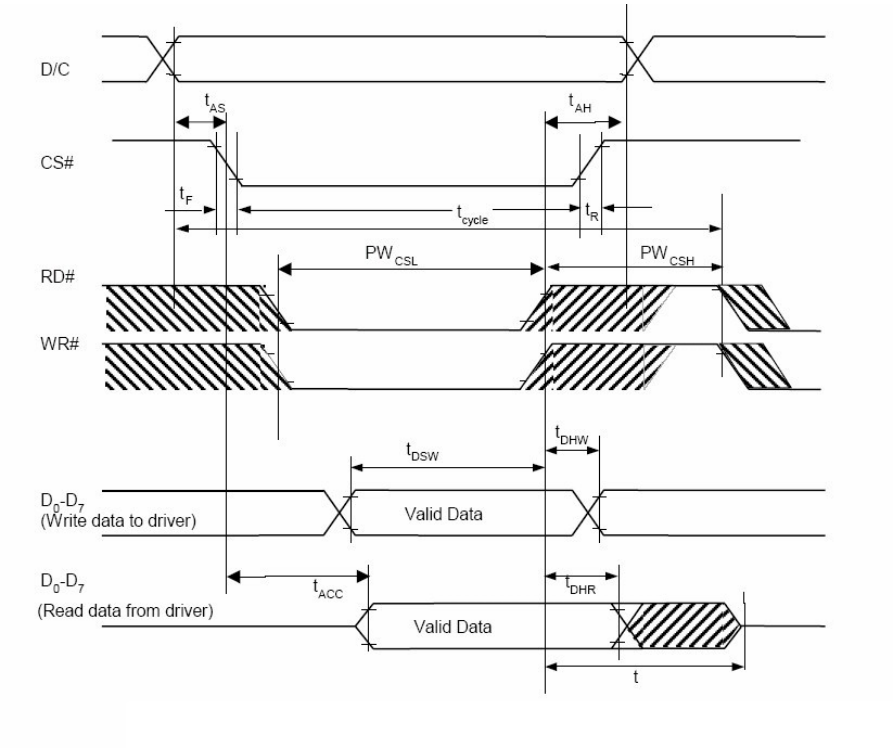
5.1.11.1 Parallel Interface Timing Characteristics:

Parallel Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tcycle	300	-	-	ns
Address Setup Time	tAS	0	-	-	ns
Address Hold Time	tAH	0	-	-	ns
Write Data Setup Time	tDSW	40	-	-	ns
Write Data Hold Time	tDHW	7	-	-	ns
Read Data Hold Time	tDHR	20	-	-	ns
Output Disable Time	tOH	-	-	70	ns
Access Time	tACC	-	-	140	ns
Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	PW CSL	120 160	-	-	ns
Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	PWCSH	60 60	-	-	ns
Rise Time	tR	-	-	15	ns
Fall Time	tF	-	-	15	ns
Frame Frequency	tFRM	70	75	85	Hz



Parallel Interface Timing Diagram for 68 Series MPU

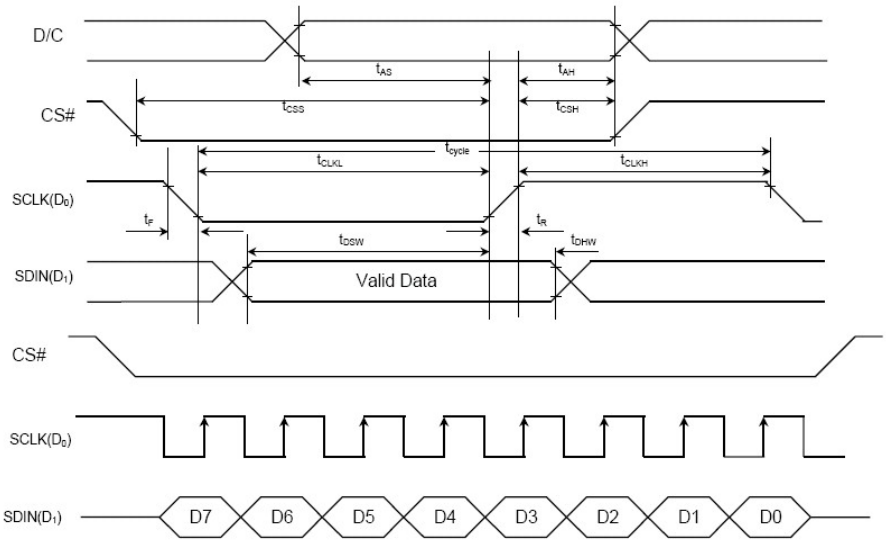


Parallel Interface Timing Diagram for 80 Series MPU

5.1.11.2 Serial Interface Timing Characteristics:

Serial Interface Timing Characteristics

Description	Symbol	Min.	Typ.	Max.	Unit
Clock Cycle Time	tcycle	250	-	-	ns
Address Setup Time	tAS	150	-	-	ns
Address Hold Time	tAH	150	-	-	ns
Chip Select Setup Time	tCSS	120	-	-	ns
Chip Select Hold Time	tCSH	60	-	-	ns
Write Data Setup Time	tDSW	100	-	-	ns
Write Data Hold Time	tDHW	100	-	-	ns
Clock Low Time	tCLKL	100	-	-	ns
Clock High Time	tCLKH	100	-	-	ns
Rise Time	tR	-	-	15	ns
Fall Time	tF	-	-	15	ns
Frame Frequency	tFRM	70	75	85	Hz



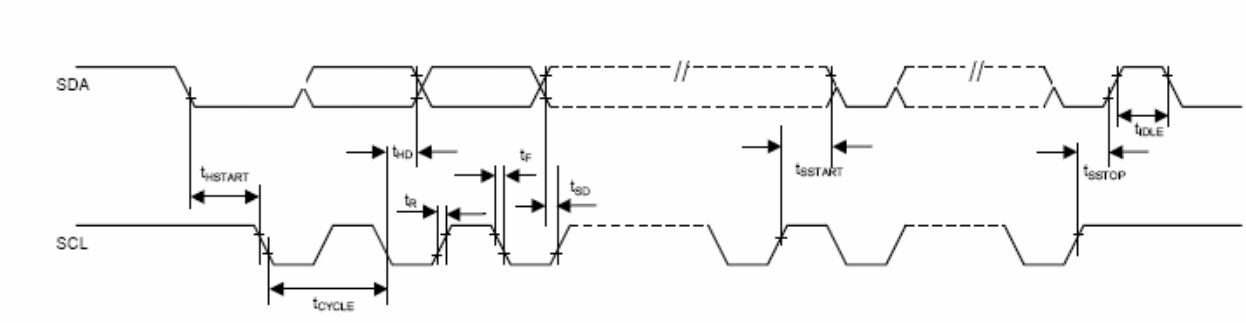
Serial Interface Timing Diagram

5.1.11.3 I²C Interface Timing Characteristics:

I²C Interface Timing Characteristics

(V_{DD}-V_{SS}=2.4 to 3.5V, T_A=-40 to 85° C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



I²C Interface Timing Diagram

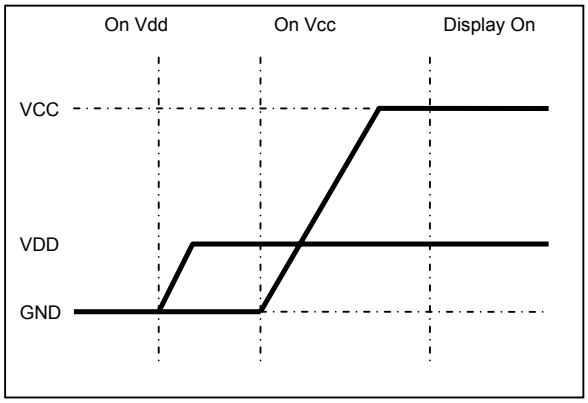
5.2 Display Programming

5.2.1 Power Up and Down Sequence

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

5.2.1.1 Power-Up Sequence:

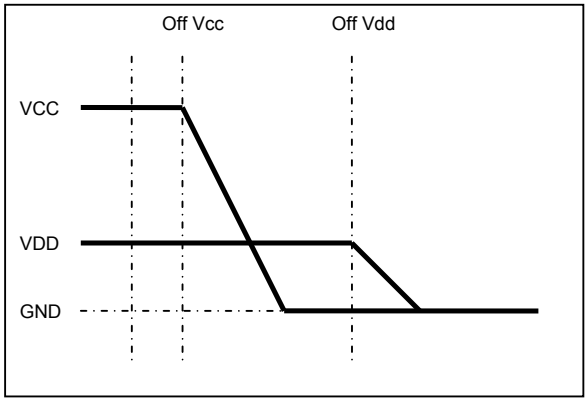
I. Power-Up Vdd and wait until stable
II. Hardware reset
III. Send display off command
IV. Power-Up Vcc
V. Delay 100ms (when Vcc is stable)
VI. Send Display on command



Power Up Diagram

5.2.1.2 Power-Down Sequence:

I. Send Display off command
II. Power down Vcc
III. Delay 100ms (when Vcc is reach 0 and panel is completely discharges)
IV. Power down Vdd



Power Down Diagram

5.2.4 Recommended Initialization Command

Command at VDD = 3.0V, VCC = 9.0V, Frame frequency = 100 Hz

Refer to IC specification: Solomon SSD1303/SSD0303 OLED/PLED Segment/Common Driver with Controller CMOS. After power up, the commands specified in table below must be executed during initialization.

Initialization Sequence

Command	Code	Default	Initialization For Module		
Set Lower Column Address		00	04		
Set Higher Column Address		10	12		
Set Horizontal Scroll Setup	26		(1)		
Set Activate Horizontal Scroll			2F(2)		
Set Deactivate Horizontal Scroll			2E(3)		
Set Contrast Control	81	80	15 (7) (*)	2B (8) (*)	30(9) (*)
Set Brightness For Color Banks	82	80	Default		
Set Look Up Table (LUT) For Area Color	91		(4)		
Set Bank Color Of For Bank 1-16 (Page 0)	92		(5)		
Set Bank Color Of For Bank 17-32 (Page 1)	93		(6)		
Set Segment Re-map		A0	A1		
Set Display Start Line		40	Default		
Set Display Offset	D3	00	Default		
Set Multiplex Ratio	A8	3F	0F		
Set Entire Display ON / OFF		A4	default		
Set Normal / Inverse Display		A6	default		
Set Display On/Off		AE	AF		
Set Page Address		B0-B7	B0-B1		
Set COM Output Scan Direction		C0	C8		
Set Clock Divide	D5	70	72		
Set Area Color Mode ON / OFF	D8	00	default		
Set Pre-Charge Period	D9	22	default		
Set COM Pins Hardware Configuration	DA	12	default		
Set VCOM Level	DB	35	04 (7) (*)	0F (8) (*)	34(9) (*)
			Single Supply (VDD) - Internal VCC		
Set DC-DC ON / OFF	AD	8B	Default		
			Dual Supply (VDD, VCC) - External VCC		
Set DC-DC ON / OFF	AD	8B	8A		

(*). This setting represents maximum luminance for proper operation of the display. Lower setting can be used for dimming. Higher setting will adversely affect the operating lifetime as defined in this specification.

(1). This command is used to setup the horizontal scrolling.

(2). This command is used to activate the horizontal scrolling.

(3). This command is used to deactivate the horizontal scrolling.

(4, 5, 6).This command is not used (A different kind of Area color mode)

(7). Elegance Yellow Product
(8). Elegance Yellow (High Luminance), Lime Green, Tiger Orange, and Golden Orange Products
(9). Galaxy White and Ocean Blue Products

5.2.5 Sample Initialization Code

```
/*****************************************
// Hilo H36XX Initialization Command
******************************/
// Lower Column Address
   WriteCommand(0x04);    /* Set Lower Column Address */
// High Column Address
   WriteCommand(0x12);    /* Set Higher Column Address
                          */
// Display Start Line
   WriteCommand(0x40);    /* Set Display Start Line */
// Contrast Control Register
   WriteCommand(0x81);    /* Set Contrast Control */
   WriteCommand(0x2B);    /* 0 ~ 127 (1) */
// Re-map
   WriteCommand(0xA1);    /* [A0]:column address 0 is
                          map to SEG0 , [A1]: column
                           address 131 is map to SEG0*/
// Entire Display ON/OFF
   WriteCommand(0xA4);    /* A4=ON */
//  Normal or Inverse Display
    WriteCommand(A6);      /* Normal Display*/
// Multiplex Ratio
   WriteCommand(0xA8);    /* Set Multiplex Ratio */
   WriteCommand(0x0F);    /* Set to 16 Mux*/
// Set DC-DC
   WriteCommand(0x8A);    /* Set DC-DC */
                          /* 8B=ON, 8A=OFF */
// Display ON/OFF
   WriteCommand(0xAF);    /* AF=ON , AE=OFF*/
// Display Offset
   WriteCommand(0xD3);    /* Set Display Offset */
   WriteCommand(0x00);    /* No offset */
// Display Clock Divide
   WriteCommand(0x72);    /* Set Clock Divide */
                          /* Set to 150Hz */
// Area Color Mode
   WriteCommand(0xD8);    /* Set Area Color On or Off       */
  WriteCommand(0x00);     /* Mono Mode */

// COM Pins Hardware Configuration
   WriteCommand(0x12);    /* Set  Pins Hardware
                          Configuration */
// VCOMH
   WriteCommand(0xDB);    /* Set VCOMH (2) */
   WriteCommand(0x0F);
```

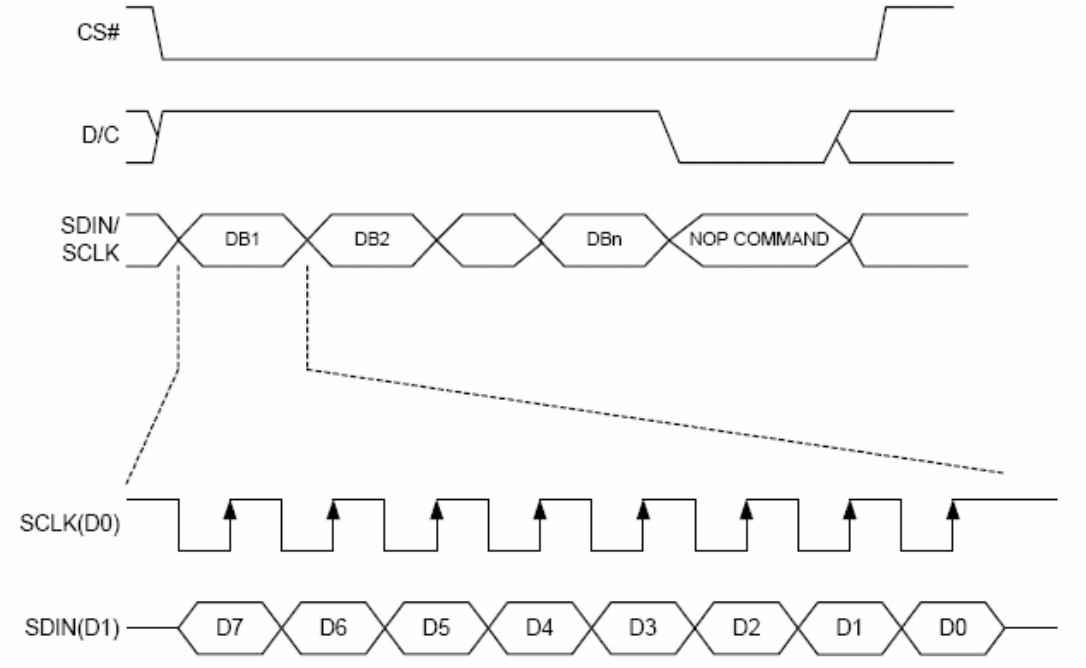
NOTE : The code for initialization command above is valid with reference to Table of Initialization Sequence.

5.2.6 MPU Serial Interface

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In ISPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 pin should be left open. D3 to D7, E and R/W pin can be connected to external ground.

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6 … D0. D/C# sampled on every eighth clock and the data byte in the shift register is written to the Display Data RAM command register in the same clock.

During data writing, an additional NOP command should be inserted before the CS# goes high.



Display data write procedure in SPI mode

Note: Below is the sample command to be inserted before the CS# goes high.

```
for (i=0;i<96;i++)    /* 96 COLUMN */
{
WriteData(0xFF);   /*ALL PIXEL ON */
}
WriteCommand(0xE3);  /* NOP COMMAND */
```

5.3 Optical Characteristics:
(Ta = 25°C, unless otherwise stated)

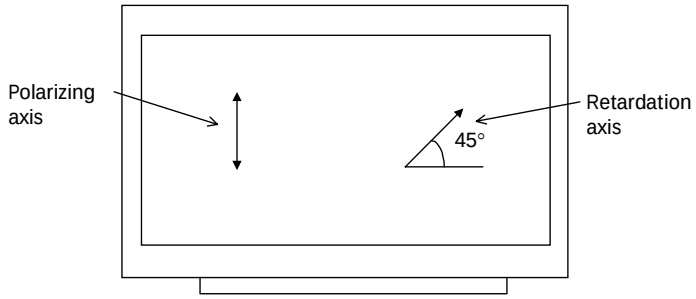
Optical & Operating Lifetime Characteristics

	Condition	Min.	Typ.	Max.	Unit
Contrast Ratio	$\theta = \phi = 0°$, Dark	-	2000	-	-
	Direct Sun Light	1.05	-	-	
Brightness Uniformity	$\theta = \phi = 0°$	-	-	+20	%
Visible Flicker	$\theta = \phi = 0°$	-	None	-	-
Cross Talk (Brightness variation of non-selected pixels)	$\theta = \phi = 0°$	-	-	10	%

Product	Color	X color coordinate, 1931CIE ±0.02	Y color coordinate, 1931CIE ±0.02	Initial Luminance, cd/m²			Operating Life*, hour, @ 25°C
				Min.	Typ.	Max.	
H3600-OS096016PP08MW1B10	Galaxy White	0.245±0.030	0.250	70	80	90	3.5K
H3610-OS096016PP08MB2B10	Ocean Blue	0.140	0.170	20	30	40	3.5K
H3650-OS096016PP08MY0B10	Elegance Yellow	0.460	0.540	90	100	140	40K
H3650-OS096016PP08MY0B10 Programmed to higher luminance	Elegancce Yellow	0.460	0.540	180	200	280	10K
H3665-OS096016PP08MG1B10	Lime Green	0.370	0.620	100	120	140	10K
H3675-OS096016PP08MO1B10	Tiger Orange	0.630	0.370	40	50	60	10K
H3672-OS096016PP08MO2B10	Golden Orange	0.600	0.400	50	60	70	10K

*Operating Lifetime is Time to Half Luminance; based on the display operated at 25°C at typical brightness level with specified software settings, until 50% of initial luminance is reached.

5.3.1 Polarizing Angle:

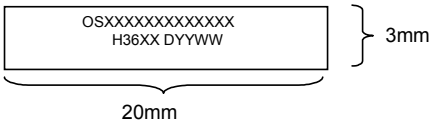


Orientation of OLED polarizer angle

5.3.2 Mechanical Characteristics:

5.3.1.1 Interconnections: The display module should be electrically connected to the user's board by soldering or hotbar reflow.

5.3.1.2 Product Marking: Parts are marked with a label on the module



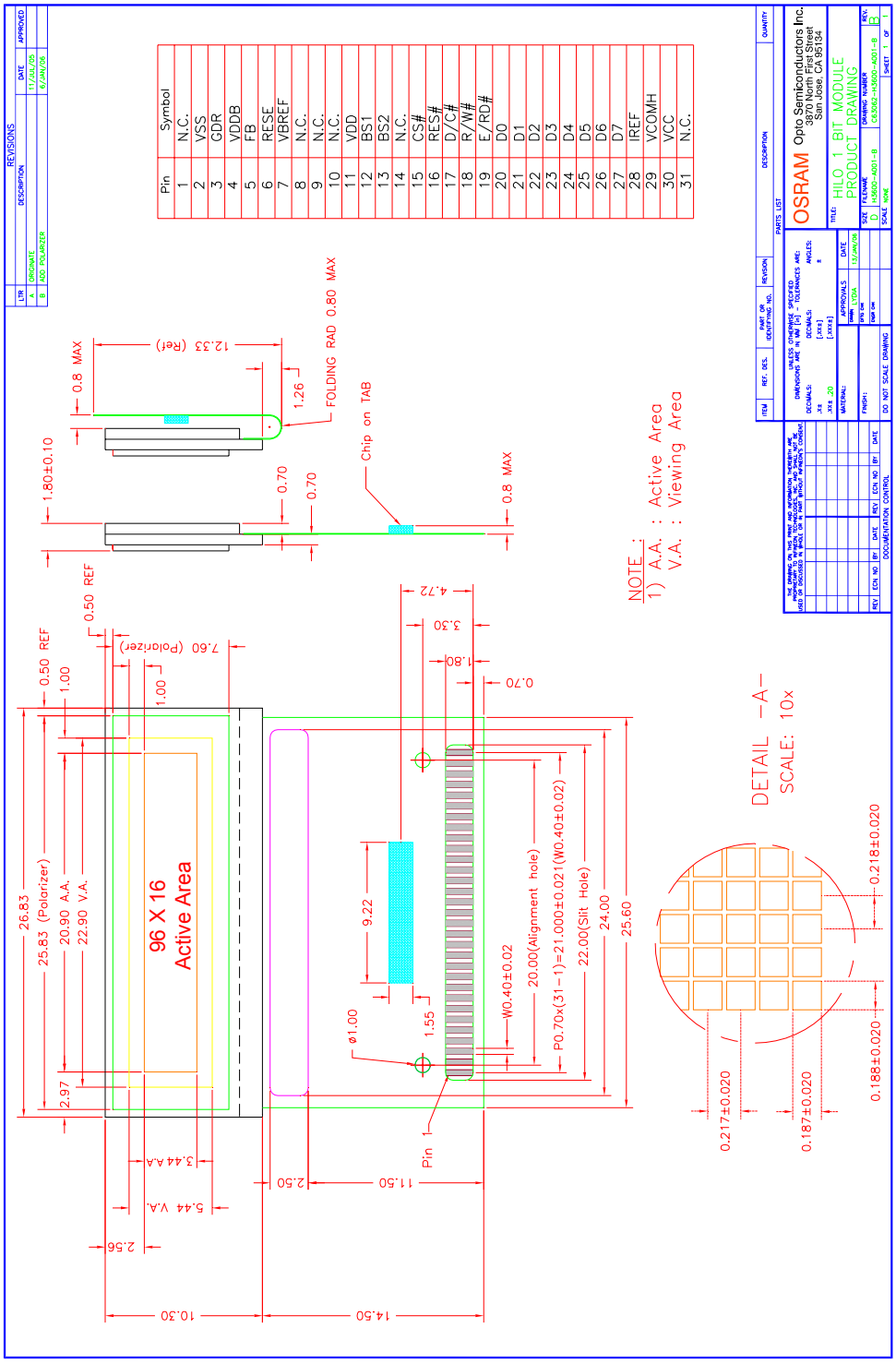
Legend
OSRAM P/N & Code
Date Code
D: Day; YY: Year
WW: PC Week
YY: Fiscal Year

Description of part label marking requirement

5.4 Module Mechanical Drawings:

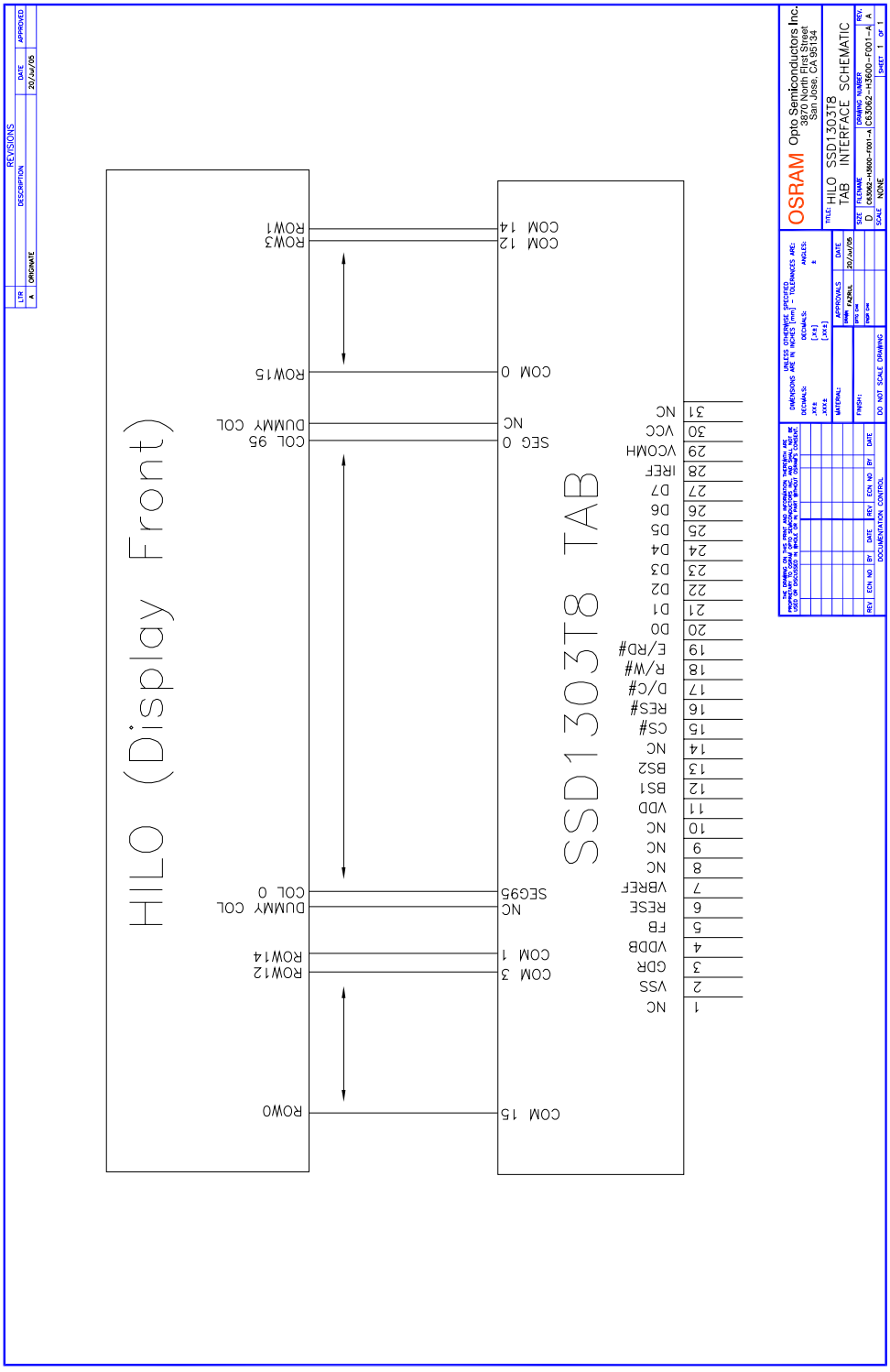
The mechanical drawing shown in below Figure is for reference.

Hilo Module drawing



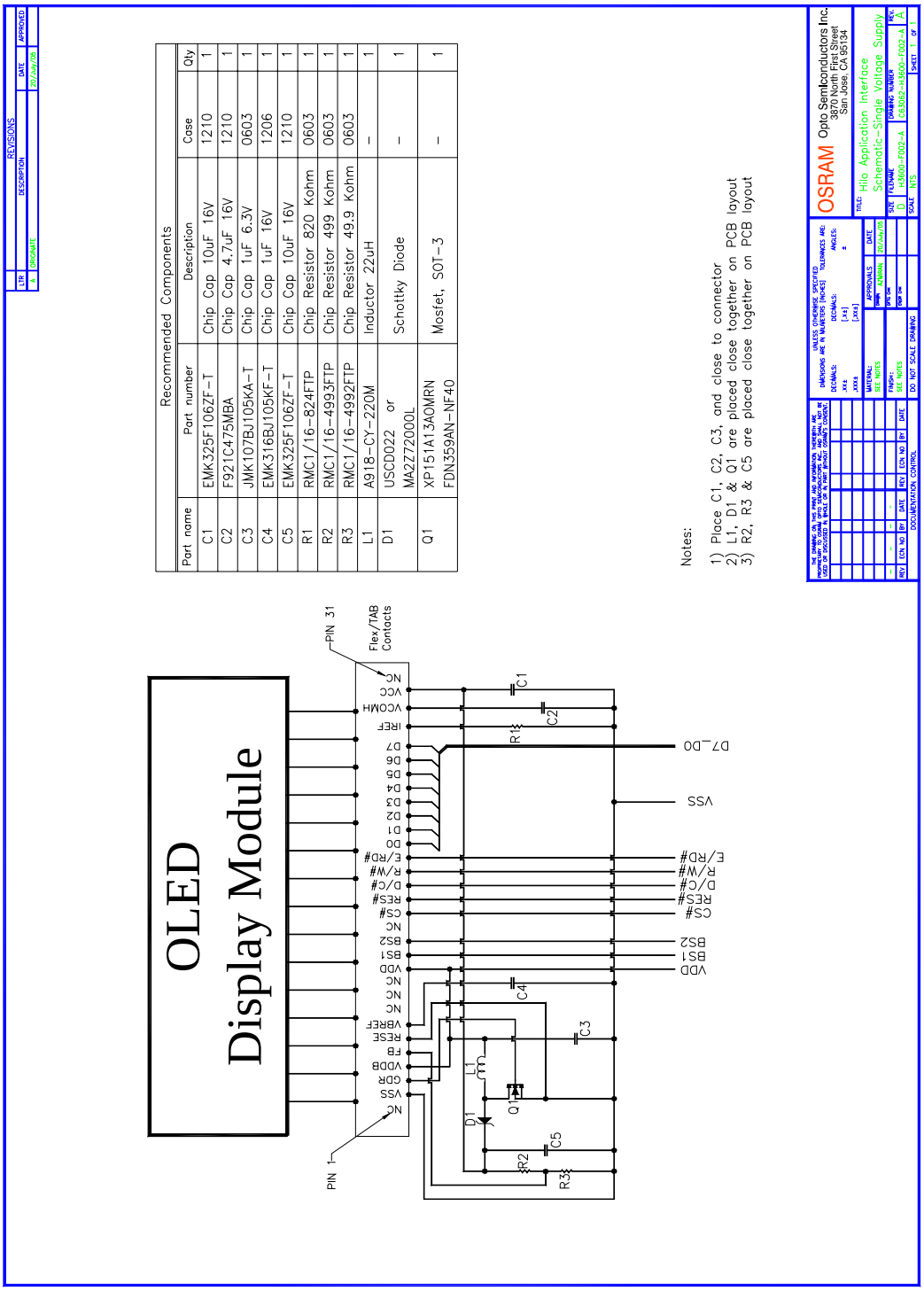
6. Schematic Drawing

Hilo SSD0303 TAB Interface Schematic

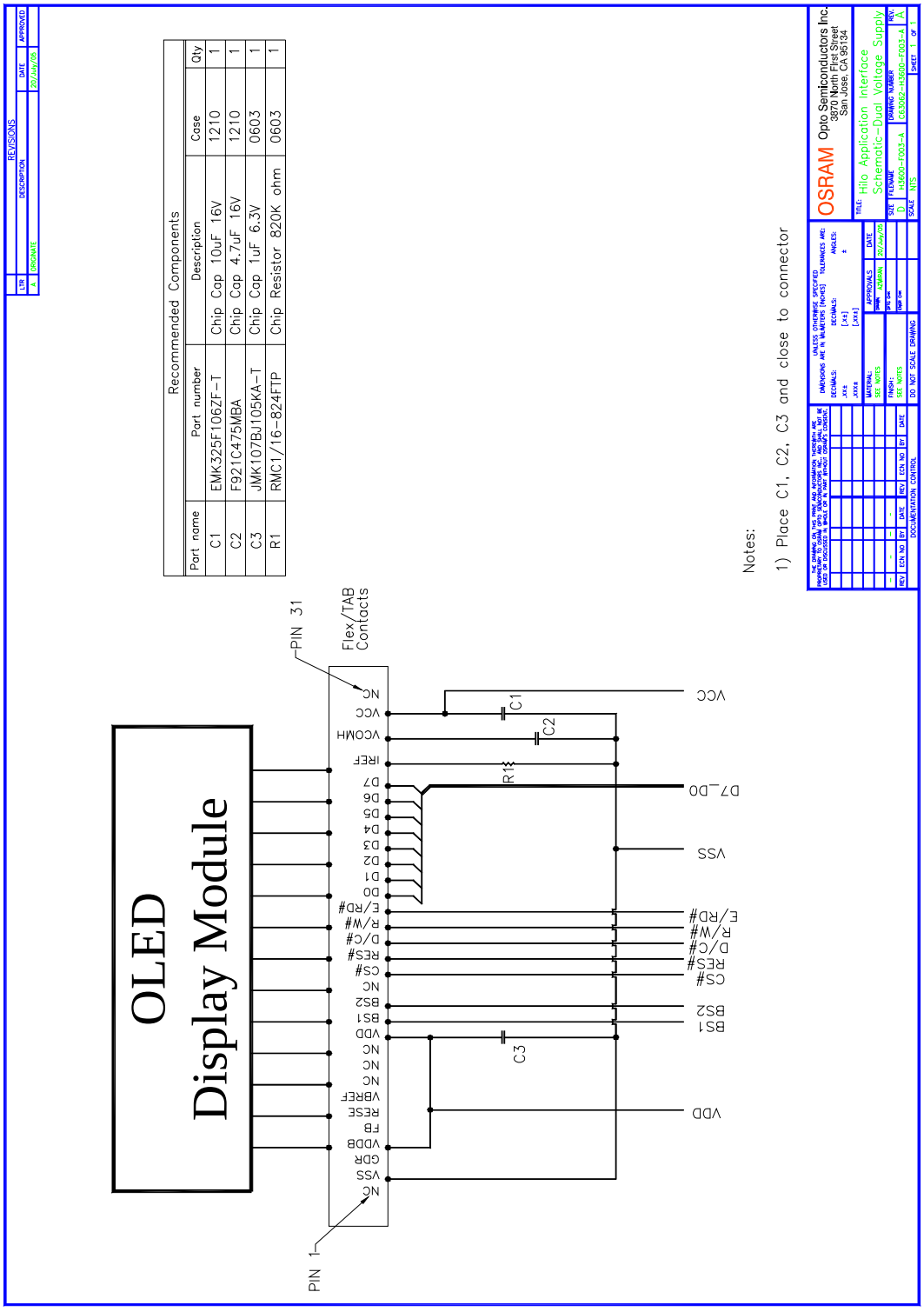


Remarks : SSD0303 is labeled with SSD1303T8 on TAB

Hilo Application Interface Schematic – Single Voltage Supply



Hilo Application Interface Schematic – Dual Voltage Supply



7. Qualification Tests:

For reference, the main qualification tests and test criteria done on the OLED module are indicated in below tables.

OLED Module Internal Qualification Tests

Test	Condition	Duration	
		Elegance Yellow, Light Green, Tiger Orange, Golden Orange, Lime Green	Galaxy White/ Ocean Blue
High Temperature and Humidity Bias (THB)*	60°C / 90% RH	250 hrs	-
High Temperature Operating (ELT)*	70°C	336 hrs	-
High Temperature and Humidity unbiased (THS)*	60°C / 90% RH	-	250 hrs unbiased
Powered Temperature Cycle (PTC)*	-30°C / 70°C; 30 min. dwell time; 15 min. transition time	60 cycles	
Thermal Shock (TSK)	-40°C / 85°C; 45 min. dwell time; 15 sec. Transition time	100 cycles	
Low Temperature Storage (LTS)	-40°C	336 hrs	
High Temperature Storage (HTS)	70°C	336 hrs	
Low Air Pressure LAT **	15kPa 25°C (0.15bar)	16hrs	
Mechanical Vibration **	10-58hz 0.75mm 58-150Hz 10g, 1oct/min	10 sweeps per X, Y, Z direction	
Mechanical Shock **	11ms half sine 100g peak	6 shocks per X, Y, Z direction	
Mechanical Bump **	6ms half sine 40g Peak	1000 bumps per X, Y, Z direction	

* ***Note 1:*** The modules are powered for these tests, with a standard OSRAM pattern (50% emission ratio)

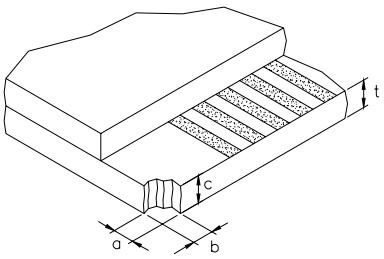
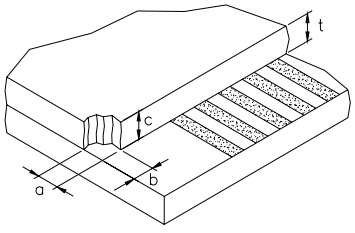
** ***Note 2***: These mechanical tests may not be performed on the specific part numbers in this specification.

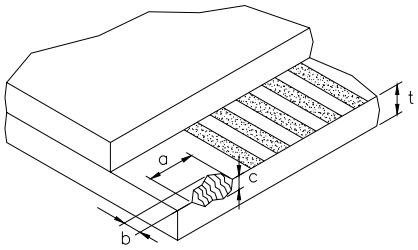
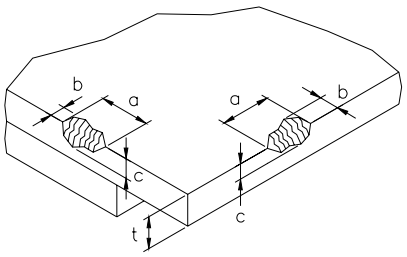
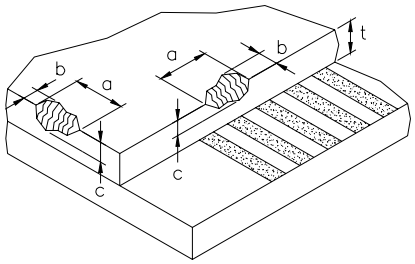
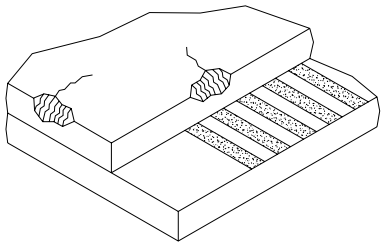
OLED Module Qualification Test Criteria

Acceptance Criteria (without polarizer):	Test Patterns for Powered Tests:
< 50% luminance loss after test 5 point luminance uniformity <20% No mechanical failure No electrical failure Pixel gap (initial + growth) ≤ 30%	Checkerboard pattern Inverse Checkerboard pattern All pixels On All pixels Off

8. COSMETIC CRITERIA:

<table>
<tr><th>Items</th><th>Criterion for Defects</th><th>Defect Type</th></tr>
<tr><td>Black / bright spot, particle, pin-hole (on the glass / polarizer), dent on polarizer</td><td>Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.1</td><td>Not counted</td></tr><tr><td>0.1 ≤ Φ ≤ 0.2</td><td>3</td></tr><tr><td>Φ > 0.2</td><td>0</td></tr></table>* Φ = (Long diameter + Short diameter)/2</td><td>Minor</td></tr>
<tr><td>Scratches / lines on the polarizer</td><td>Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>W≤ 0.1</td><td>Not counted</td></tr><tr><td>L ≤ 2, 0.1 < W ≤ 0.2</td><td>3</td></tr><tr><td>W > 0.2</td><td>0</td></tr></table></td><td>Minor</td></tr>
<tr><td>Polarizer Bubble</td><td>Reject if bubble is observed with naked eyes at 30cm distance. with the following criteria

Within Viewing Area
<table><tr><th>Size Φ (mm)</th><th>Acceptable number</th></tr><tr><td>Φ ≤ 0.2</td><td>Not counted</td></tr><tr><td>0.2≤Φ ≤ 0.3</td><td>3</td></tr><tr><td>0.3 < Φ</td><td>0</td></tr></table>Outside Viewing Area – IGNORE</td><td>Minor</td></tr>
<tr><td>Polarizer coverage</td><td>Reject if the polarizer does not cover the Viewing Area.</td><td>Minor</td></tr>
<tr><td>Corner Chip</td><td>Criteria for Corner Chip
t = Glass thickness
Accept If
a ≤ 1.5 mm or
b ≤ 1.5 mm
c ≤ t
  </td><td>Minor</td></tr>
<tr><td>Corner Chip</td><td>Accept If
a ≤ 3.0 mm
or
b ≤ 3.0 mm
  </td><td>Minor</td></tr>
</table>

Chip on contact pad	**Criteria for Chips on contact pad** t = Glass thickness Accept if b ≤ 1/3 width of contact ledge 	Minor
Chip on Face of Display	**Criteria for Chips on Face of Display** Accept if b ≤ 1.5mm 	Minor
Chip on Back of Display	**Criteria for Chips on Back of Display** Accept if b ≤ 3.0 mm 	Minor
Chip with crack	**No crack allowed** 	Major

Definition of W & L & ϕ (Unit: mm)

Note: Distance between any two defects should be over 5 mm

9 General OLED Module Handling & Care

9.1 Mechanical Handling

9.1.1 Avoid mechanical stress, such as shock and pressure. For parts designed without bezel, exercise caution to avoid glass chipping. When handled with bare fingers, pay special attention to sharp glass edges to avoid potential injury.

9.1.1 Avoid touching TAB contact pad with bare fingers.

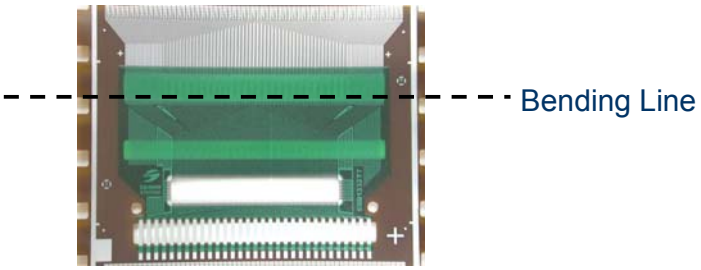
9.1.2 Handle the polarizer with care. Avoid hard or sharp objects in contact with the display surface.

9.1.3 Store and operate the OLED display within the specified ratings. It is recommended to store them as they have been contained in the inner container at the time of delivery from us.

9.1.4 Installation Bending: The flex is generally designed to facilitate mounting to a PCB or connector. It is not a dynamic flex. Therefore, bending should be limited to less than 10 times.

9.1.5 Bending Radius: The minimum bending radius is as shown in the product drawing or equal to the thickness of the rear cap glass, whichever is smaller.

9.1.6 TAB/TCP: Some designs have area with base polyimide layer removed (Slit) with exposed copper traces unsupported. The flex can be bent much easier at this location for installation (non-dynamic) as shown in below Figure.



TAB bending line

9.1.7 Wipe off saliva or water drops immediately. Contact with water over a long period of time may cause damage of polarizer or color fading, while an active OLED display with water condensation on its surface will cause corrosion of metal traces.

9.1.8 Cleaning: Use non-abrasive cloth or applicator (dipped in IPA or ethanol if necessary) to gently wipe over the surface of the display. Do not submerge the module into any kind of solvent or any other chemicals like acids, bases and salts.

9.2 ESD

9.2.1 Electrostatic discharge (ESD): OLED modules are semiconductor devices. Take ESD handling precautions by wearing a ground strap and avoid contacting electrical connections.

Condition	MM	HBM
Vdd mode	200v	2000v
Vss mode	200v	2000v
IO mode	200v	2000v

9.3 Solderibility (TAB, COF)

9.3.1 Hotbar reflow: 260°C(**) for 5 seconds (max.)
Manual soldering: at each contact, 260°C(**) for 3 seconds (max.)
Use only soldering iron with proper grounding connection
ACF: Refer to ACF material supplier recommendations, but not exceeding hotbar reflow conditions.

TAB flex can be soldered only one time. Rework of TAB soldering can cause broken conductive traces of the flex.

(**) Perceived temperature at contact pads