Elementary CMOS Circuits

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CMOS Circuit Fabrication

The basic processes of integrated circuit fabrication in a foundry are

- Wafer preparation
- Oxidation
- Deposition
- Lithography and etching
- Epitaxy, diffusion, and ion implantation

The designer of integrated circuits ought to be familiar with these processes in order to understand the project steps and the design rules and to be able to modify the operations that violate these rules. This chapter contains a brief description of the basic processes listed above. The reader can find more about this technology in [12, 16, 60].

1.1 WAFER PREPARATION

CMOS technology uses single-crystal silicon wafers for integrated circuit fabrication. Wafers are silicon disks 75 mm to 230 mm in diameter. Silicon in its poly-crystal form is obtainable from sand. In the wafer production process, the level of natural impurities is lowered and other substances are added, in strictly controlled amounts, to obtain the single-crystal form with the required electrical properties. Wafers are less than 1 mm thick and are sliced from cylindric ingots pulled from silicon melt in the process known as the Czochralski method. One face of the wafer, on which the integrated circuit will be built, is polished before further operation.

Professor Jan Czochralski, a Polish scientist, published his method in the German journal "Zeitschrift für physikalische Chemie" in 1918. However, he was known mainly for "Bahnmetal" (the metal for train bearings), which was strategic material in Germany during the First World War. This invention made him a rich man. He came back to Poland after the rebirth of the state. In Poland, he was able to very effectively combine his the scientific work with activity in industry. His excellent career ended with the Second World War.

1.2 OXIDATION

Silicon dioxide (SiO_2) is the natural insulator material of the silicon-based semiconductor industry. As can be seen in Fig.2.1, which shows the structure of a transistor, during oxidation it is important to obtain a very thin film of so-called gate oxide where the gate will be laid and the transistor will be located. Thin layers of SiO_2 are covered by patterned photoresist and another layer of dioxide is grown. The patterned regions are covered by gate oxide and are called active areas, whereas the remaining area is covered by field oxide.

1.3 DEPOSITION, LITHOGRAPHY AND ETCHING

Lithography and etching are processes similar to those known from photographic techniques. They are used in order to obtain necessary patterns in films. The film materials are usually silicon dioxide (SiO_2), silicon nitride (SiN), polysilicon (polycrystalline silicon), photoresist (photoresistive organic material) and metal (aluminum and occasionally copper). These materials are deposited on the wafer. Chemical vapor deposition (CVD) is a frequently used deposition technique.

Optical photholitography, which uses ultraviolet light, is the common technique used to obtain patterns in a photoresist. The layer deposited on the wafer and not protected by the photoresist is etched by appropriate chemicals. For higher resolution of the lithography process, an electron beam or an X-ray source can be used instead of an ultraviolet light source.

1.4 EPITAXY, DIFFUSION, AND ION IMPLANTATION

Silicon in the single-crystal form is an insulator. Two kinds of impurities, acceptors and donors, are introduced into this material in order to obtain a conducting p-type and n-type material, respectively. Epitaxy, diffusion, and ion implantation processes are used for the introduction of impurities.

- The epitaxial layer is obtained during the epitaxial growth. The CVD technique is used in the process. Epitaxial layers are usually used in bipolar transistor fabrication.
- Diffusion is the method most frequently used for doping silicon in chosen areas of the wafer. Impurities diffuse from the layer deposited on the surface into the silicon and inside the silicon between areas with different concentrations of dopants. This kind of migration also takes place in integrated circuits at normal operating temperatures. However, it takes tens of years for natural migration to become significant.
- In the ion implantation method, ionized impurities are accelerated and lodged in the substrate. Dopant concentration (in the substrate) depends on the velocity and density of the ionized impurity beam. This method ensures good control of dopant concentration.

1.5 CONTACTS AND INTERCONNECTS

Interconnects between elements of a circuit are etched in polysilicon and metal films. Polysilicon is used for gate electrodes of transistors and for short interconnects. Connections through isolating layers are called contacts (connections between metal and doped silicon) or vias (connections between metal layers).

1.6 MASKS AND DESIGN RULES

Photolithography is used in manufacturing integrated circuits. Hence, the description of mask geometries for all lithography processes ought to be the result of integrated circuit design. It is easy to obtain such description using current computer systems called silicon compilers. Masks described in a given format (usually the Caltech Intermediate Format or CIF is used) are sent to a foundry where a laser beam or an electron beam are used to produce actual masks.

In order to illustrate the use of masks in the fabrication of CMOS circuits, let us describe an n-well, single-poly, double-metal process. The description of the process is simplified and some intermediate steps are omitted in order to emphasize the role of each mask. The process is as follows:

00 start with p-type wafer,

01 diffuse n-well, mask: *01*, **nwell**,

02 grow gate oxide,

03 define active area, mask: *02*, **active**,

04 grow field oxide,

05 deposit polysilicon,

06 pattern polysilicon, mask: *03*, **poly**,

07 implant n^+ dopants, mask: *04*, **nplus**,

08 implant p^+ dopants, mask: *05*, **pplus**,

09 pattern contact openings, mask: *06*, **contact** ,

10 deposit metal 1,

11 pattern metal 1, mask: *07*, **metal1**,

12 deposit oxide (CVD),

13 pattern metal 2 contacts, mask: *08*, **via**,

14 deposit metal 2,

15 pattern metal 2, mask: *09*, **metal2**,

16 deposit glass (nitride passivation),

17 pattern pad openings, mask: *10*, **pad**.

Minimum sizes of the patterns on the masks depend on the resolution of the lithography and on the features of the technology process. The set of geometrical specifications of patterns is called the design rules. The process specific design rule set contains all dimensions in microns and can be applied in a particular fabrication process only. A more general approach is scaling, in which a generic metric λ is used. All dimensions are given in multiples of λ, which makes the layout independent of the fabrication process. When the process is chosen, λ assumes a value; for example $0.2\mu m$ in the 0.4 CMOS process.

Basic design rules are shown in Fig.1.1. The minimum widths, spacings and other dimensions shown in Fig.1.1 (in multiples of λ and in microns for a hypothetical 0.4 CMOS p-substrate (n-well) process) are as follows:

w1 n-well width, $w1 = 6\lambda = 1.2\mu m$,

w2 n-well spacing, $w2 = 5\lambda = 1\mu m$,

w3 n-well spacing to n-plus (p-plus), $w3 = 6\lambda = 1.2\mu m$,

d1 n-plus (p-plus) width, $d1 = 3\lambda = 0.6\mu m$,

d2 n-plus (p-plus) spacing, $d2 = 3\lambda = 0.6\mu m$,

p1 polysilicon width, $p1 = 2\lambda = 0.4\mu m$,

p2 polysilicon spacing, $p2 = 2\lambda = 0.4\mu m$,

p3 polysilicon spacing to n-plus (p-plus), $p3 = 1\lambda = 0.2\mu m$,

p4 polysilicon overhang (extension of gate), $p4 = 2\lambda = 0.4\mu m$,

c1 contact dimension, $c1 = 2\lambda = 0.4\mu m$,

c2 contact spacing, $c2 = 2\lambda = 0.4\mu m$,

c3 metal enclosure of contact, $c3 = 1\lambda = 0.2\mu m$,

m1 metal width, $m1 = 3\lambda = 0.6\mu m$,

m2 metal spacing, $m2 = 4\lambda = 0.8\mu m$.

Complete design rules can be obtained from the foundries in technological files, in a format suitable for tools used by designers of integrated circuit layouts.

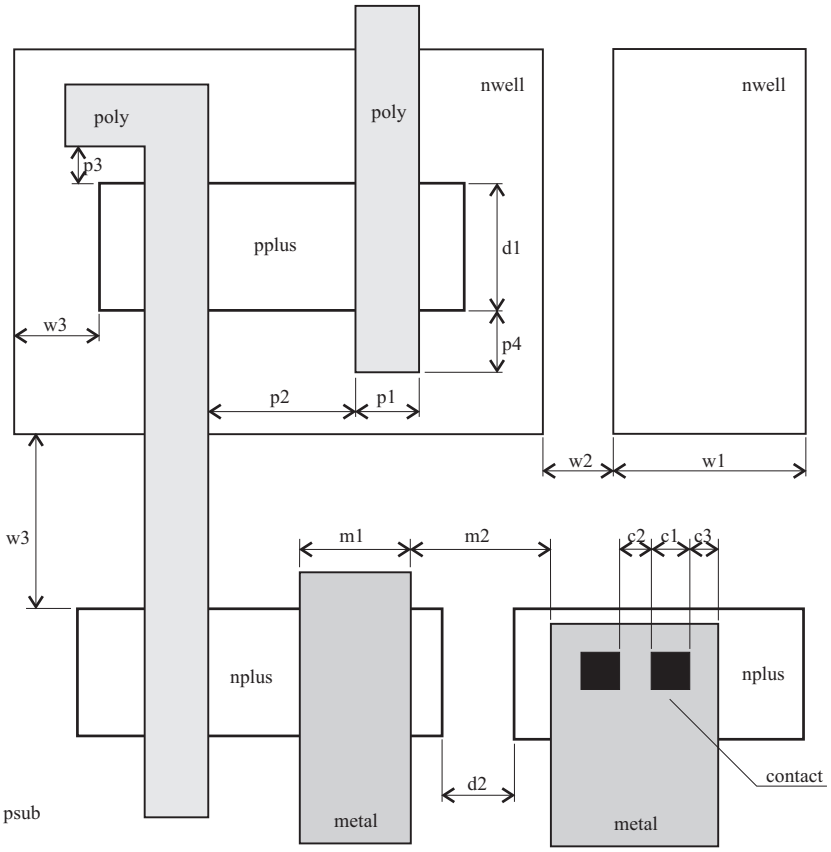


Fig. 1.1 Example of design rules.

Fig.1.2 shows the layout of the inverter from Fig.2.15, illustrating the above design rules. The lengths of transistor channels are many times greater than their widths. Hence, the transistors are laid out as folded devices. The use of folded transistors is characteristic of analog cells in which such channel dimensions are typical. In Fig.1.2, the transistor Mp is folded three times and Mn is folded once. In comparison to unfolded transistors, folded devices have smaller areas of drains and sources, which decreases parasitic effects. Polysilicon, depicted by the shaded area, forms the gates of the transistors and is used as the connection between the gates and the input. The areas of the sources and drains are not visible in Fig.1.2. Their location is indicated by black boxes, which are contacts with p-plus and n-plus regions. The metal V_{DD} line has additional contacts with the n-well area.

1.7 PROBLEMS

1. Using the design rules for a hypothetical 0.4 CMOS p-substrate (n-well) process, draw a layout of the switch in Fig.2.10, assuming that the widths and lengths of transistor channels are as small as possible.

2. Draw a layout of the Schmitt trigger shown in Fig.2.19, for a hypothetical 0.4 CMOS p-substrate (n-well) process. Assume that widths of pMOS transistor channels are $24\mu m$ and nMOS are $8\mu m$, whereas all channel lengths are $4\mu m$.

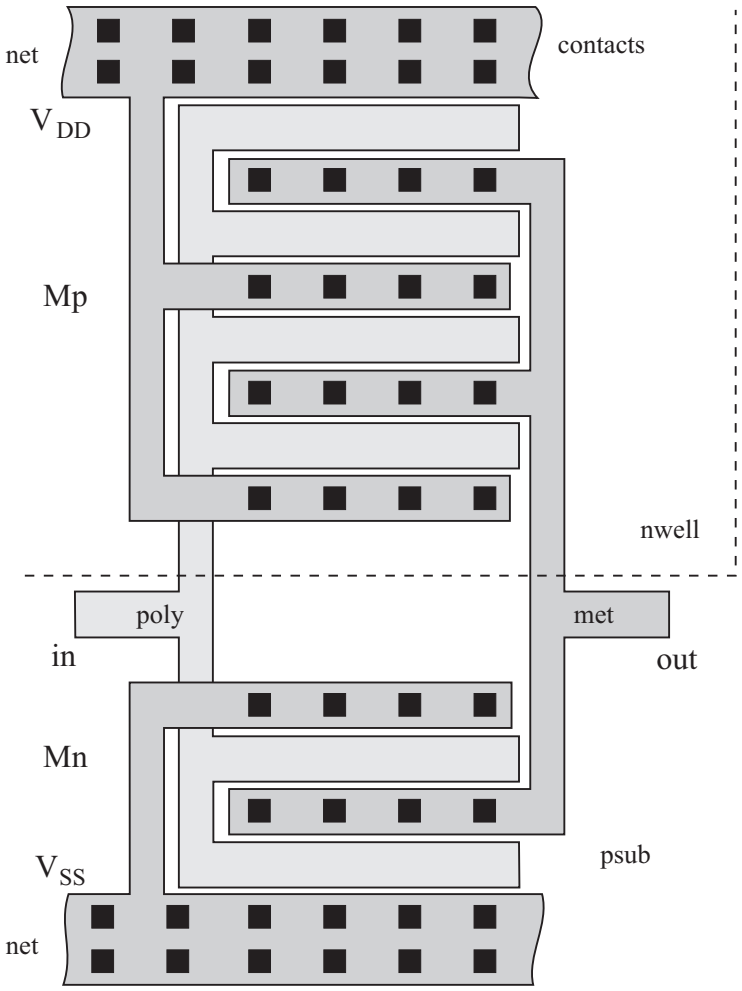


Fig. 1.2 Example of inverter layout.

2

Properties of Basic CMOS Cells

CMOS VLSI circuits, introduced in the 1960s, have since become the dominant silicon technology. In comparison to other technologies, the main advantages of CMOS technology are

- A small number of fabrication processes
- High layout density
- Reduced power consumption

These advantages make CMOS circuits low cost and very attractive on the market.

This chapter describes the properties of MOS transistors used to realize all basic cells of integrated circuits. Operation, performance, and design of these cells are also presented in this chapter.

2.1 CMOS TRANSISTOR CHARACTERISTICS

MOS transistors are the simplest active element of integrated circuits. MOS transistors were invented by J. E. Lilienfeld (between 1925 and 1932 he got several patents in Canada and US) and by O. Heil (the first English patent for such a transistor was issued in 1935). However, it was the rapid development of technology in the early 1960s that allowed implementation of MOS transistors and their use on a wide scale.

An n-channel MOS transistor is presented in Fig.2.1. Two n^+ regions obtained by diffusion in p-type silicon (substrate) are called drain and source. The polysilicon gate is isolated from the p-type silicon by a thin gate oxide layer with the thickness x_{ox} less than a few hundredths of a micrometer. The process of obtaining such a device is described in the next chapter. Voltages are delivered to drain, source, and gate by metal (Al) contacts denoted as black boxes. The current flow I_D from drain to source is controlled by the drain-source voltage V_{DS}, the gate-source voltage V_{GS}, and the source-bulk voltage V_{SB}. Usually, there is a short circuit between the source and the bulk ($V_{SB} = 0$). In this case, the current I_D is controlled by voltages V_{DS} and V_{GS}, and the transistor can be in a cutoff mode ($I_D = 0$) or in an active mode ($I_D \neq 0$), depending on the parameter called the threshold voltage, V_{Tn}. When $V_{GS} \leq V_{Tn}$, the transistor is *off* (cutoff), and when $V_{GS} > V_{Tn}$, the transistor is *on* (active). In the cutoff mode, one of the pn junctions between substrate and drain or source is reverse-biased and the current I_D does not flow. In the active mode, the positive gate potential induces the conducting channel between drain and source. The channel is an electron surface with the length equal to L and the width equal to W. The section of a MOS transistor in Fig.2.1 shows only the channel length. The channel width is perpendicular to the figure plane. Because of the type of the channel, the transistor is called $nMOS$. The $pMOS$ transistor is complementary to $nMOS$, which means that the current flows in the opposite direction and the voltages are reversed. The technology which exploits the $nMOS/pMOS$ pair of transistors is called the CMOS technology. In Fig.2.2 different symbols of $nMOS$ and $pMOS$ transistors are presented. Let us note that we can use either complete symbols, which show four device electrodes, or simplified symbols, in which the bulk electrode is omitted. When the simplified symbols are used, the bulk electrode of an $nMOS$ is

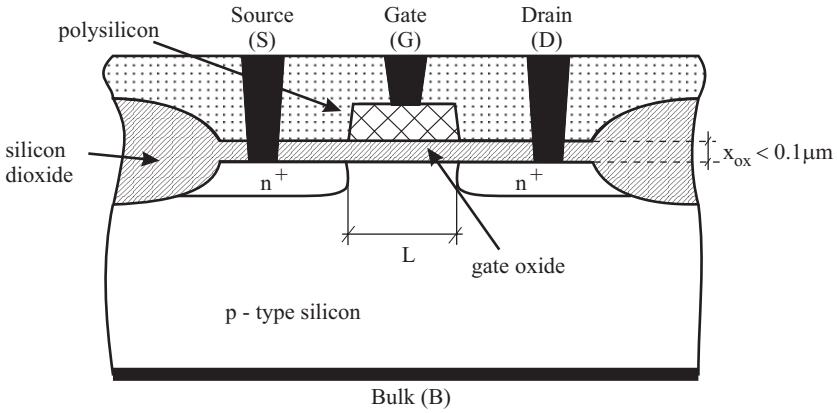


Fig. 2.1 An n-channel MOS transistor.

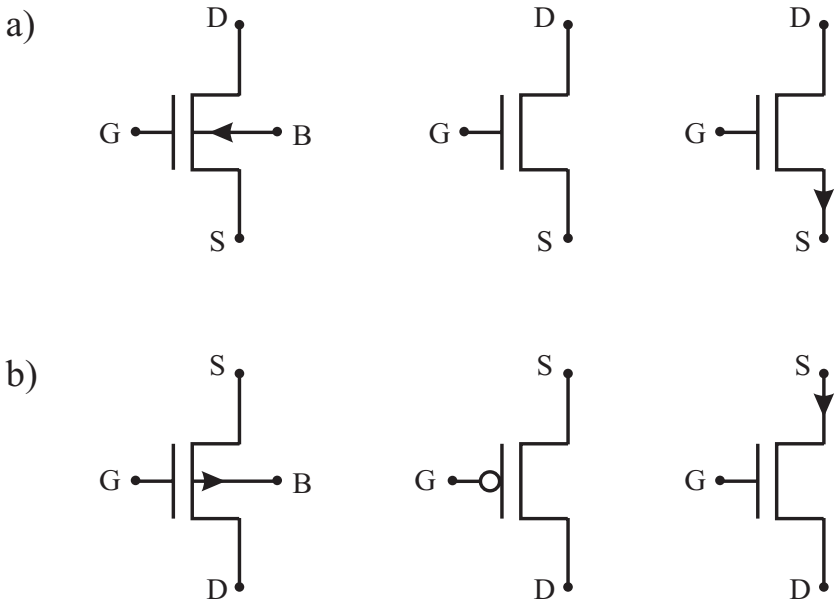


Fig. 2.2 MOS transistor symbols: a) nMOS, b) pMOS.

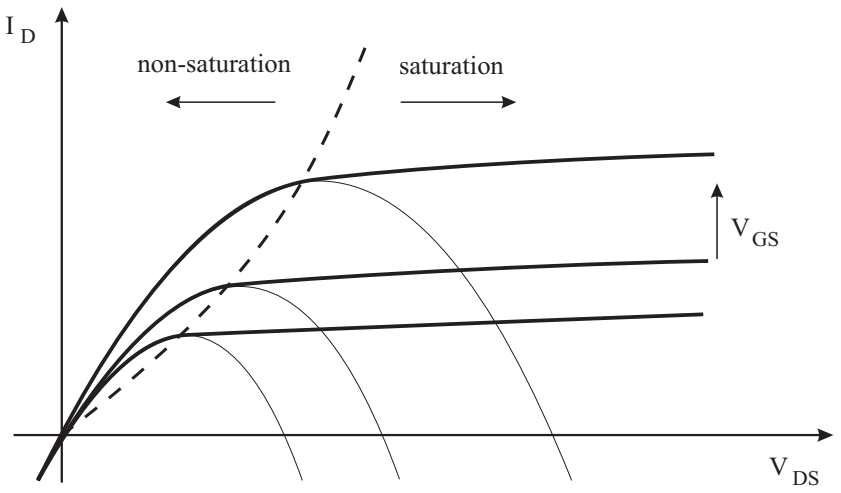


Fig. 2.3 nMOS transistor current-voltage characteristic.

assumed to be connected to the negative power supply (or to the ground) and that of a $pMOS$ to the positive power supply.

Because the $nMOS$ and $pMOS$ transistors are complements of each other, we will examine the current-voltage characteristics of an $nMOS$ transistor only. The simplest model is the square-low one, in which it is assumed that the drain current depends on drain-source voltage V_{DS} in the first and second power,

$$I_{Dn} = \frac{\beta_n}{2}[2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2], \tag{2.1}$$

exclusively. It is obvious that the device transconductance β_n is proportional to the width W and inversely proportional to the length L of the transistor channel and can be expressed as

$$\beta_n = k_n' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}, \tag{2.2}$$

where k_n' is described by physical parameters:

- μ_n - the electron mobility, (μ_p - hole mobility for pMOS transistors),
- C_{ox} - the oxide capacitance per unit gate area.

The unit area oxide capacitance can be calculated from

$$C_{ox} = \frac{\epsilon_{ox}}{x_{ox}}, \tag{2.3}$$

where $\epsilon_{ox} = 3.9\epsilon_0$, $\epsilon_0 = (8.854E - 14)F/m$, and x_{ox} is the gate oxide thickness.

The coefficient of the first component in the formula (2.1) is linearly dependent on the gate-to-source voltage V_{GS}. For a given voltage V_{GS}, equation (2.1) describes the parabola shown in Fig.2.3. Only the part of the parabola between the origin of the coordinate system and the peak current of the parabola is used as the current-voltage characteristic. We say that when the values of current and voltages are in this region, the transistor is in a non-saturated mode. It is easy to calculate from the extreme condition, $I_{Dn}'(V_{DS}) = 0$ that the saturation voltage has the value

$$V_{DS,sat} = V_{GS} - V_{Tn}, \tag{2.4}$$

for which the value of current is

$$I_{Dn} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2. \tag{2.5}$$

A more exact relation for the current in the saturated mode is in the form

$$I_{Dn} = \frac{\beta_n}{2}(V_{GS} - V_{Tn})^2[1 + \lambda_n(V_{DS} - V_{DS,sat})], \tag{2.6}$$

as it is shown in Fig2.3, where λ_n is the n-channel-length modulation parametr. The dashed line in Fig.2.3 denotes the border between saturated and non-saturated areas.

The equation of a pMOS transistor in the non-saturated mode can be written in the following form, complementary to (2.1):

$$I_{Dp} = \frac{\beta_p}{2}[2(V_{SG} + V_{Tp})V_{SD} - V_{SD}^2], \tag{2.7}$$

where the current is oriented as shown in Fig.2.2, the threshold voltage V_{Tp} now has a negative value, and $V_{GS} = -V_{SG} < V_{Tp}$. Similarly, in the saturated mode we have:

$$I_{Dp} = \frac{\beta_p}{2}(V_{SG} + V_{Tp})^2, \tag{2.8}$$

or

$$I_{Dp} = \frac{\beta_p}{2}(V_{SG} + V_{Tn})^2[1 + \lambda_p(V_{SD} - V_{SD,sat})], \tag{2.9}$$

where

$$V_{SD,sat} = V_{SG} + V_{Tp}. \tag{2.10}$$

2.2 MODELING

Integrated circuit simulators, such as Spice, Eldo, or Saber, use more complex MOS transistor models than those that were described in the previous section. The parameters introduced so far, i.e.

- Transconductance parameter k'_n or k'_p
- Threshold voltages V_{Tn} and V_{Tp}
- Carrier mobility μ_n or μ_p
- Gate-oxide thickness x_{ox}
- Channel-length modulation parameter λ

are used on almost all levels of complexity of transistor models. The additional parameters that describe parasitic capacitors and parasitic resistors are very important, too. Parasitic capacitors of a MOS transistor are shown in Fig.2.4a. In order to calculate their capacitances, the technology parameters shown in Fig.2.4b are used at all levels of models. These parameters, and their units, are as follows:

- C_{GSO} - gate-source overlap capacitance/channel width, $[F/m]$,
- C_{GDO} - gate-drain overlap capacitance/channel width, $[F/m]$,
- C_{GBO} - gate-bulk overlap capacitance/channel length, $[F/m]$,
- C_{j0} - zero-bias junction bottom capacitance/source (drain) area, $[F/m^2]$,
- C_{jsw} - zero-bias junction sidewall capacitance/source (drain) perimeter length, $[F/m]$.

The gate-bulk overlap capacitance, C_{GBO}, cannot be shown in the cross-section presented in Fig.2.4.

The parameters are introduced with the use of a command that in Spice, for example, has the form

$$\textbf{.model} \quad < model \;\; name > \quad \textbf{nmos} \;\; [model \;\; parameters] \tag{2.11}$$

for an NMOS transistor, or

$$\textbf{.model} \quad < model \;\; name > \quad \textbf{pmos} \;\; [model \;\; parameters] \tag{2.12}$$

for a PMOS one.

The following examples

$$\begin{aligned} \textbf{.model} \quad & model1 \;\; \textbf{nmos} \;\; \textbf{level} = 2 \;\; \textbf{nsub} = 20E+16 \\ + \quad & \textbf{ld} = 0.05u \;\; \textbf{tox} = 8n \;\; \textbf{kp} = 170u \;\; \textbf{vto} = 0.5 \\ + \quad & \textbf{uo} = 400 \;\; \textbf{lambda} = 0.01 \\ + \quad & \textbf{cgso} = 0.2n \;\; \textbf{cgdo} = 0.2n \;\; \textbf{cgbo} = 0.1n \\ + \quad & \textbf{cj} = 0.9m \;\; \textbf{cjsw} = 0.3n \;\; \textbf{rsh} = 80 \end{aligned} \tag{2.13}$$

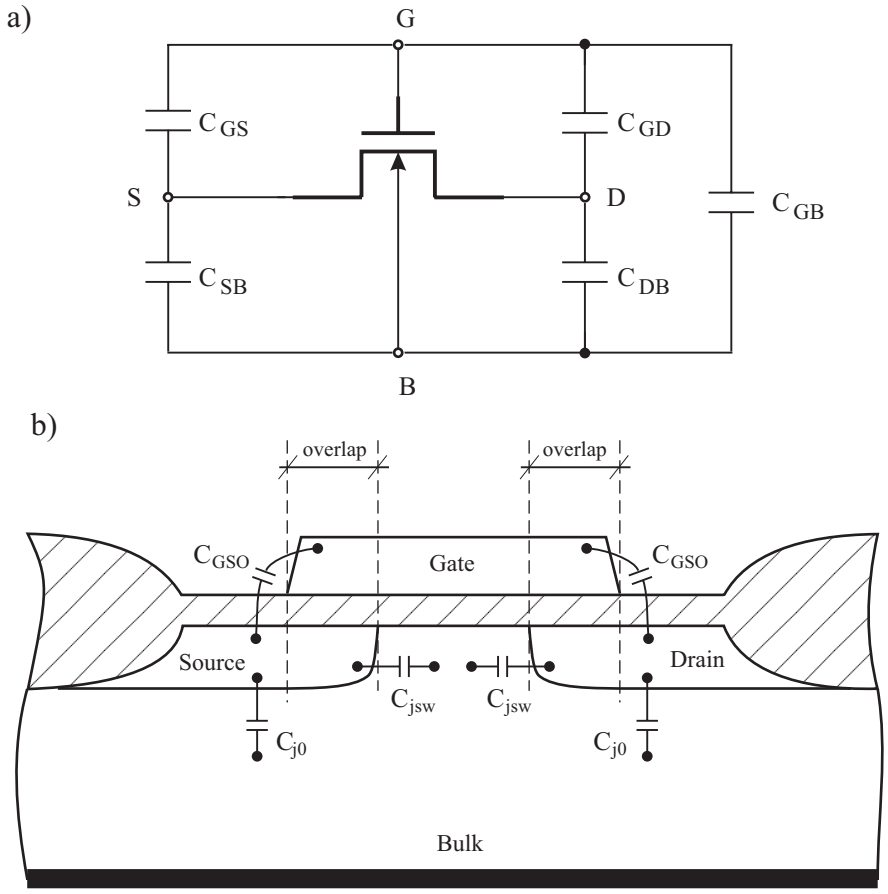


Fig. 2.4 Parasitic capacitors, (a), and technology parameters of a MOS transistor, (b).

$$
\begin{array}{rl}
\textbf{.model} & model2\ \ \textbf{pmos}\ \ \textbf{level} = 2\ \ \textbf{nsub} = 10E+16 \\
+ & \textbf{ld} = 0.05u\ \ \textbf{tox} = 8n\ \ \textbf{kp} = 60u\ \ \textbf{vto} = -0.6 \\
+ & \textbf{uo} = 140\ \ \textbf{lambda} = 0.03 \\
+ & \textbf{cgso} = 0.2n\ \ \textbf{cgdo} = 0.2n\ \ \textbf{cgbo} = 0.1n \\
+ & \textbf{cj} = 1.2m\ \ \textbf{cjsw} = 0.4n\ \ \textbf{rsh} = 160
\end{array} \tag{2.14}
$$

describe some parameter values typical for a $0.4\mu m$ p-substrate (n-well) CMOS process, where

level model selector,

nsub substrate doping concentration, $[cm^{-3}]$,

ld length of lateral diffusion l_0, $[m]$,

tox oxide thickness x_{ox}, $[m]$,

kp transconductance coefficient k'_n or k'_p, $[A/V^2]$,

vto zero-bias threshold voltage V_{Tn} or V_{Tp}, $[V]$,

uo surface mobility μ_n or μ_p, $[cm^2/V \cdot sec]$,

lambda channel-length modulation parameter λ, $[V^{-1}]$,

cgso gate-source overlap capacitance C_{GSO}, $[F/m]$,

cgdo gate-drain overlap capacitance C_{GDO}, $[F/m]$,

cgbo gate-bulk overlap capacitance C_{GBO}, $[F/m]$,

cj zero-bias junction bottom capacitance C_{j0}, $[F/m^2]$,

cjsw zero-bias junction sidewall capacitance C_{jsw}, $[F/m]$,

rsh drain or source diffusion sheet resistance R_{sh}, $[\Omega/square]$.

In Spice, MOS transistor description has the general form

$$
\begin{array}{rl}
\textbf{M} < name > & < drain\ \ node > \ < gate\ \ node > \ < source\ \ node > \\
+ & < bulk/substrate\ \ node > \ < model\ \ name > \\
+ & [\textbf{l} =< value >]\ \ [\textbf{w} =< value >] \\
+ & [\textbf{ad} =< value >]\ \ [\textbf{as} =< value >] \\
+ & [\textbf{pd} =< value >]\ \ [\textbf{ps} =< value >] \\
+ & [\textbf{nrd} =< value >]\ \ [\textbf{nrs} =< value >] \\
+ & [\textbf{nrg} =< value >]\ \ [\textbf{nrb} =< value >] \\
+ & [\textbf{m} =< value >]
\end{array} \tag{2.15}
$$

where

l channel length, $[m]$,

w channel width, $[m]$,

ad drain diffusion area, $[m^2]$,

as source diffusion area, $[m^2]$,

pd drain diffusion perimeter, $[m]$,

ps source diffusion perimeter, $[m]$,

nrd relative drain resistivity, $[squares]$,

nrs relative source resistivity, [*squares*],

nrg relative gate resistivity, [*squares*],

nrb relative substrate resistivity, [*squares*],

m device multiplier, simulating parallel devices.

This description allows to calculate parasitic capacitors and resistors on the basis of given channel dimensions and drain and source areas and perimeters. The following examples

$$\begin{aligned} \mathbf{M}n1 \quad & 2\ \ 1\ \ 3\ \ 3\ \ model1\ \ \mathbf{l} = 0.4u\ \ \mathbf{w} = 1.2u \\ + \quad & \mathbf{ad} = 2.4p\ \ \mathbf{as} = 2.4p\ \ \mathbf{pd} = 6.4u\ \ \mathbf{ps} = 6.4u \\ + \quad & \mathbf{nrd} = 10\ \ \mathbf{nrs} = 10\ \ \mathbf{nrg} = 8 \end{aligned}$$

and

$$\begin{aligned} \mathbf{M}p1 \quad & 2\ \ 1\ \ 4\ \ 4\ \ model2\ \ \mathbf{l} = 0.4u\ \ \mathbf{w} = 3.6u \\ + \quad & \mathbf{ad} = 7.2p\ \ \mathbf{as} = 7.2p\ \ \mathbf{pd} = 11.2u\ \ \mathbf{ps} = 11.2u \\ + \quad & \mathbf{nrd} = 30\ \ \mathbf{nrs} = 30\ \ \mathbf{nrg} = 24 \end{aligned}$$

illustrate the description (2.15) of $nMOS$ and $pMOS$ transistors, respectively. In these examples, the parameters from (2.13) and (2.14) are used.

2.3 SIMPLE CIRCUITS COMPOSED OF MOS TRANSISTORS

In this section, simple CMOS cells composed of one, two, or several transistors will be examined. All considerations will be based on the simplest equations given by relations (2.1), and (2.5) for an nMOS transistor and by (2.7), and (2.8) for a pMOS one. From these equations, we can obtain initial parameters of the designed cell, which can next be improved with the use of circuit simulators such as SPICE.

2.3.1 Voltage-Controlled Resistor

Transistor characteristics shown in Fig.2.3 allow us to consider a single transistor in a non-saturated mode as a nonlinear resistor controlled by the voltage V_{GS}. From (2.1) we obtain the following expression for the conductance G_{tn}:

$$G_{tn} = \frac{I_{Dn}}{V_{DS}} = \beta_n(V_{GS} - V_{Tn}) - \frac{\beta_n}{2}V_{DS}. \tag{2.16}$$

Equation (2.16) means that total conductance G_{tn} has two components corresponding to parallel resistors: a linear component $G_n = \beta_n(V_{GS} - V_{Tn})$ controlled by the voltage V_{GS} and a non-linear negative (active) one $G_{na} = -\beta_n V_{DS}/2$. The linear voltage-controlled resistor has the resistance

$$R_n = \frac{1}{G_n} = \frac{1}{\beta_n(V_{GS} - V_{Tn})}, \tag{2.17}$$

which can approximate the resitance of an $nMOS$ transistor in the non-saturated mode during simplified analysis. For the $pMOS$ transistor, from (2.7) we have the total conductance in the form

$$G_{tp} = \frac{I_{Dp}}{V_{SD}} = \beta_p(V_{SG} + V_{Tp}) - \frac{\beta_p}{2}V_{SD}, \tag{2.18}$$

and the approximate linear value of the resistor is

$$R_p = \frac{1}{\beta_p(V_{SG} + V_{Tp})}. \tag{2.19}$$

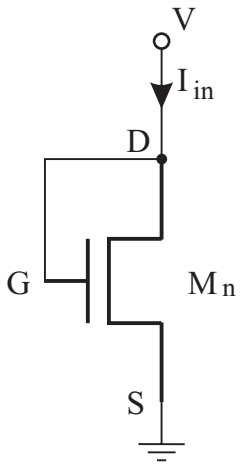


Fig. 2.5 Diode connected nMOS transistor.

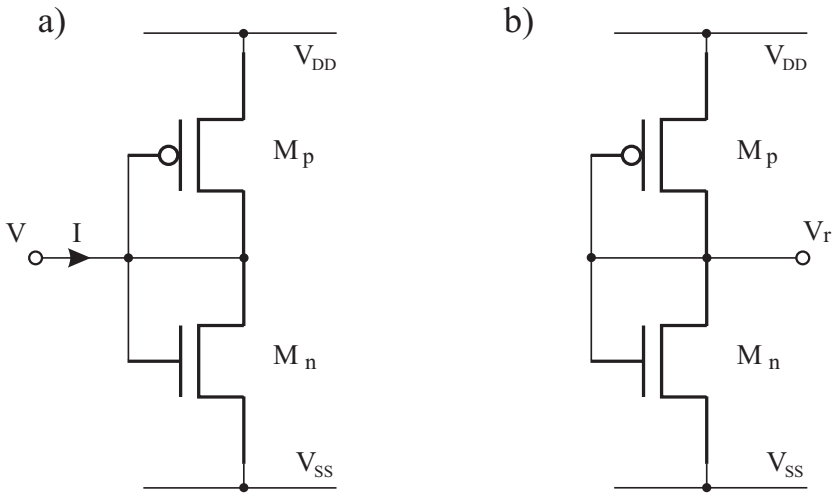


Fig. 2.6 Diode connected CMOS transistors.

2.3.2 Diode Connected Transistor

A MOS transistor with the gate and drain connected to each other is said to be diode-connected. Let us consider a diode connected $nMOS$ transistor presented in Fig.2.5. For the connection of the gate shown in this figure, the transistor is *on* if $V > V_{Tn}$ and positive current flow I_{in} is possible. If $V \leq V_{Tn}$, the transistor is *off* and the current flow is impossible, which corresponds to a reversed-biased junction.

In Fig.2.6 two complementary pairs of diode connected transistors are shown. Assuming that the transistors are in a saturated mode, we will show that the circuit in Fig.2.6a can be used as a resistor R, whereas the circuit in Fig.2.6b can be used as a voltage reference V_r. For the circuit in Fig.2.6a we have

$$I + \frac{\beta_p}{2}(V_{DD} - V + V_{Tp})^2 = \frac{\beta_n}{2}(V - V_{SS} - V_{Tn})^2, \tag{2.20}$$

and assuming

$$\beta_p = \beta_n = \beta, \tag{2.21}$$

we have

$$I = \beta(V_{DD} + V_{Tp} - V_{SS} - V_{Tn})V + \frac{\beta}{2}[(V_{SS} + V_{Tn})^2 - (V_{DD} + V_{Tp})^2]. \tag{2.22}$$

Hence

$$R = \frac{1}{\beta(V_{DD} + V_{Tp} - V_{SS} - V_{Tn})}, \tag{2.23}$$

where the parameters (2.21) are primary design variables. DC offset of the current I is given by the relation

$$I_{DC} = \frac{\beta}{2}[(V_{SS} + V_{Tn})^2 - (V_{DD} + V_{Tp})^2]. \tag{2.24}$$

Equating currents in the circuit in Fig.2.6.b, we get

$$\frac{\beta_p}{2}(V_{DD} - V_r + V_{Tp})^2 = \frac{\beta_n}{2}(V_r - V_{SS} - V_{Tn})^2, \tag{2.25}$$

and

$$V_r = \frac{\sqrt{\beta_p}(V_{DD} + V_{Tp}) + \sqrt{\beta_n}(V_{SS} + V_{Tn})}{\sqrt{\beta_n} + \sqrt{\beta_p}}. \tag{2.26}$$

Equation (2.2) shows that the parameters β_n and β_p depend on the aspect ratio W/L. According to (2.26), channel widths and lengths can be used as adjusting parameters in order to obtain the required value of the reference voltage V_r in the range $((V_{SS} + V_{Tn}), (V_{DD} + V_{Tp}))$.

2.3.3 Current Source

Considering equations (2.5, and 2.8), we see that $nMOS$ and $pMOS$ transistors in a saturated mode are ideal current sources with the current flow described by these equations. The current values depend on gate-source voltages. Equations (2.6), and (2.9) imply that in a more realistic description, the finite values of internal resistors in these sources should be taken into account. Improved performance can be obtained if two MOS transistors in cascode connection are introduced instead of a single one.

2.3.4 Switch

The MOS transistor can be in two basic modes of operation: in the active (*on*) mode and in the cutoff (*off*) one. Hence, a MOS transistor can serve as a switch. The mode of operation depends on the relation of the gate-source voltage V_{GS} with respect to the threshold voltage V_T. A switch composed of an $nMOS$ transistor is *on* when $V_{GS} > V_{Tn}$; otherwise it is *off*. A switch composed of a $pMOS$ transistor is *on* when $V_{GS} < V_{Tp}$, otherwise it is *off*. For both kinds of switches, in the *off* mode there is a high-impedance state that blocks the current flow. Therefore, the transistors can be considered as ideal switches in the *off* mode. The analysis is more complicated when the switch is on. In order to simplify the analysis, we will consider two cases of the transistor operating in the *on* mode:

1. the gate potential V_G is constant while the input voltage changes,

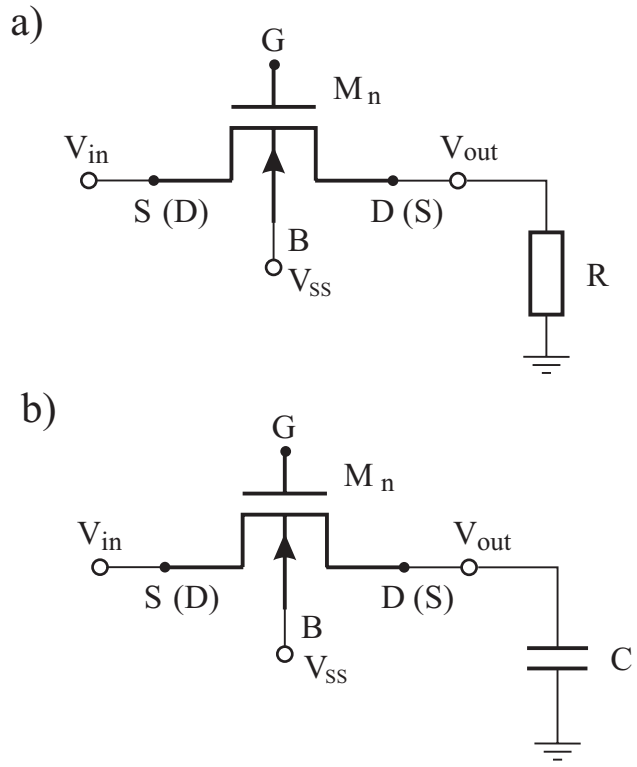


Fig. 2.7 nMOS as a switch loaded by a resistor (a), or a capacitor (b).

2. the gate potential changes (the transistor is switched *on* or *off*) and the input voltage is constant during the switching process.

In the second case, significant parasitic effects can occur.

First, let us consider a switch composed of an $nMOS$ transistor whose input is connected to an impulse voltage source. The switch can be loaded with a resistor R or a capacitor C, as shown in Fig.2.7 a and b, respectively. In the *on* mode we place high voltage $V_G = V_{DD}$ at the gate. Let us consider the switch loaded with a resistor. On the rising slope of the positive input pulse, the transistor is in the non-saturated mode and the output voltage rises. In this period V_{DS} increases, and V_{GS} decreases. When V_{DS} achieves the saturation value, $V_{DS} = V_{DS,sat} = V_{GS} - V_{Tn}$, the switch transistor reaches the saturated mode in which the value of current I_{Dn} is determined by relation (2.5). The output voltage V_{out}, shown in Fig.2.8, has its maximum value $V_{out} = I_{Dn} \cdot R$ and can be described by the equations

$$I_{Dn}R = V_{out} = \frac{\beta_n R}{2}(V_{GS} - V_{Tn})^2, \quad V_{GS} > V_{Tn}, \tag{2.27}$$

and

$$V_{out} + V_{GS} = V_{DD}. \tag{2.28}$$

We see that the transistor is in saturation during almost all time of excitation by the input source V_{in}. Similar analysis, with reversed roles of drain and source, can be performed for a negative input pulse. In this case the transistor is in a non-saturated mode for the whole input pulse duration. Hence, we use equation (2.1) of the transistor in the non-saturated mode in order to calculate the maximum value of $|V_{out}|$:

$$V_{out} = -I_{Dn}R = -\frac{\beta_n R}{2}[2(V_{GS} - V_{Tn})V_{DS} - V_{DS}^2], \quad V_{GS} > V_{Tn}, \tag{2.29}$$

where

$$V_{GS} = V_{DD} - V_{SS}, \qquad V_{DS} = V_{out} - V_{SS}. \tag{2.30}$$

A different situation occurs when the switch is loaded with a capacitor. In this case, the output voltage is described by the equation

$$I_{Dn} = C\frac{dV_{out}}{dt}. \tag{2.31}$$

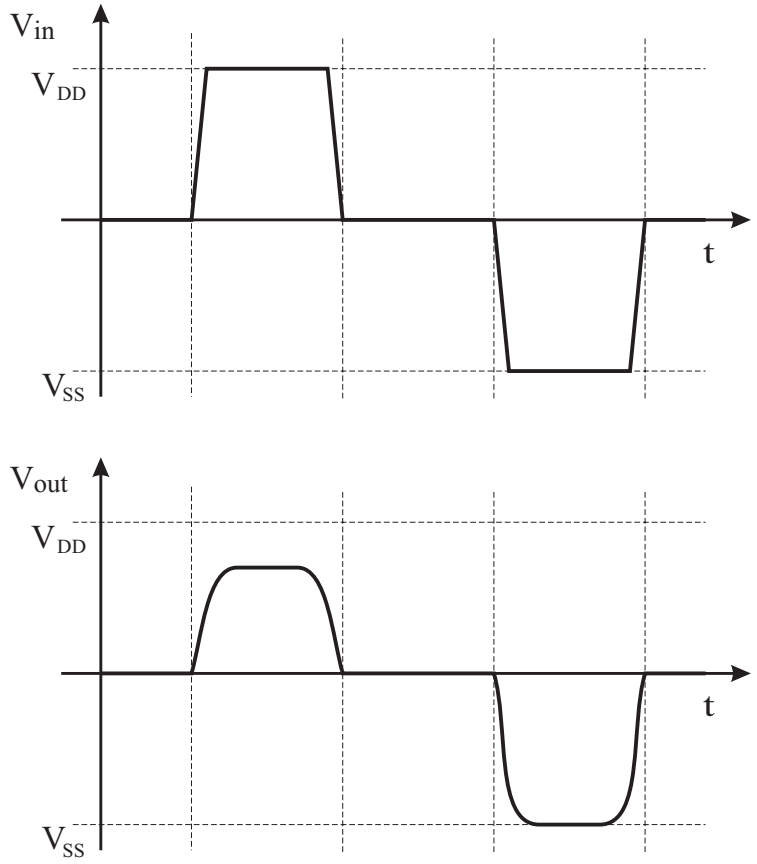


Fig. 2.8 Transient characteristics of an nMOS switch loaded by a resistor.

At the beginning of the excitation period, the transistor is in a non-saturated mode. However, after a very short time the input impulse achieves its maximum value and the transistor changes into the saturated mode. Hence, in order to determine the charging time constant we can use relations (2.5) and (2.31), which yield

$$C\frac{dV_{out}}{dt} = \frac{\beta_n}{2}(V_{DD} - V_{out} - V_{Tn})^2, \tag{2.32}$$

It is a special case of the Riccati equation

$$y' = a(t)y^2 + b(t)y + c(t), \tag{2.33}$$

which can be solved with the use of substitution

$$V_{out} = V_{DD} - V_{Tn} + \frac{1}{z}. \tag{2.34}$$

The solution which we obtain is in the form

$$V_{out} = V_{DD} - V_{Tn} + \frac{1}{A - \frac{\beta_n}{2C}t}, \tag{2.35}$$

with the integral constant A calculated from the initial condition $V_{out}(0) = 0$. Hence, the capacitor load characteristic is described by the relation

$$V_{out} = V_{DD} - V_{Tn} - \frac{V_{DD} - V_{Tn}}{\frac{t}{\tau_{ch}} + 1} = (V_{DD} - V_{Tn})\frac{\frac{t}{\tau_{ch}}}{\frac{t}{\tau_{ch}} + 1}, \tag{2.36}$$

where

$$\tau_{ch} = \frac{2C}{\beta_n(V_{DD} - V_{Tn})}. \tag{2.37}$$

In the discharge process, the current flows in the opposite direction, and the transistor, with interchanged roles of drain and source, is in the non-saturated mode in which its resistance can be estimated by the formula (2.17) with $V_{GS} = V_{DD}$. Hence,

$$\tau_{ch} = \frac{2C}{\beta_n(V_{DD} - V_{Tn})} > \tau_{dis} = \frac{C}{\beta_n(V_{DD} - V_{Tn})}, \tag{2.38}$$

as shown in Fig.2.9.

The behavior of the switch composed of a $pMOS$ transistor is complementary to a switch composed of an $nMOS$ one. Hence, the switch composed of a complementary transistor pair, presented in Fig.2.10, will have better symmetry properties. The transient characteristics of a switch composed of a complementary pair of MOS transistors is shown in Fig.2.11.

Two significant parasitic effects that have to be considered in CMOS switch operation are the clock-feed-through effect and the charge injection. These parasitic effects appear when a switch changes its mode of operation from *on* to *off* and backwards. Let us assume that the switch is controlled by the clock shown in Fig.2.12a,b. The signal Φ_1 is delivered to the gate of the $nMOS$ transistor, whereas the signal Φ_2 is delivered to the gate of the $pMOS$ transistor. Hence, the switch is *on* in the odd clock period and *off* in the even one. A so-called nonoverlapping clock (pulses of the clocks Φ_1 and Φ_2 do not overlap) with a 50% filling coefficient is used. Because of finite rise and fall times of signals, the filling coefficient is usually less than 50% in order to provide a guard interval for the proper operation of different switches in the circuit. The voltage delivered to the input of the switch is shown in Fig.2.12c, whereas the voltage on the load capacitance is shown in Fig.2.12d. When the switch is *on*, V_{out} changes exponentially, as was explained previously. In the *off* mode, the output signal is held. However, its value is not exactly the same as before the switching, as part of the charge from the transistor channels is injected into the output capacitance and not into the bulk. Glitches shown in Fig.2.12d are caused by gate capacitances, which play the role of differentiators of the clock signals. The shorter rise and fall times, the greater these parasitic effects.

2.3.4.1 CMOS Switch Logic The CMOS switch shown in Fig.2.9 can serve as a logic transmission gate (TG). Logical values 0 and 1 are associated with the low (zero) and high (V_{DD}) voltages, as will be described in detail in the next section. The symbol and the truth table of this logic device shown in Fig.2.13. The logical value from the input x_1 is transferred to the output y when $x_2 = 1$. When $x_2 = 0$, the TG is off and the output

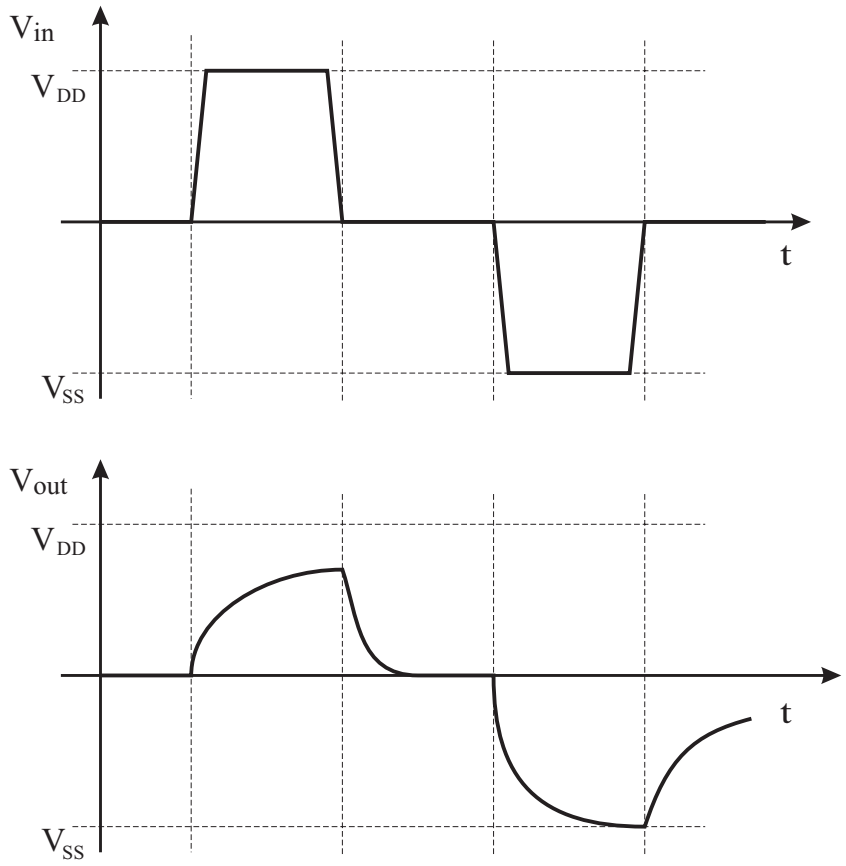


Fig. 2.9 Transient characteristics of an nMOS switch loaded by a capacitor.

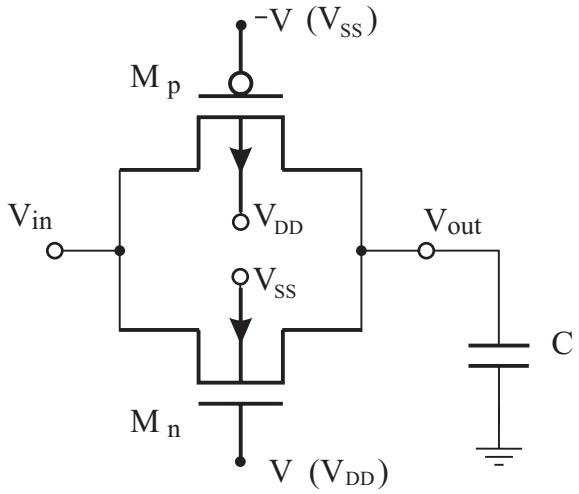


Fig. 2.10 Switch composed of CMOS transistors.

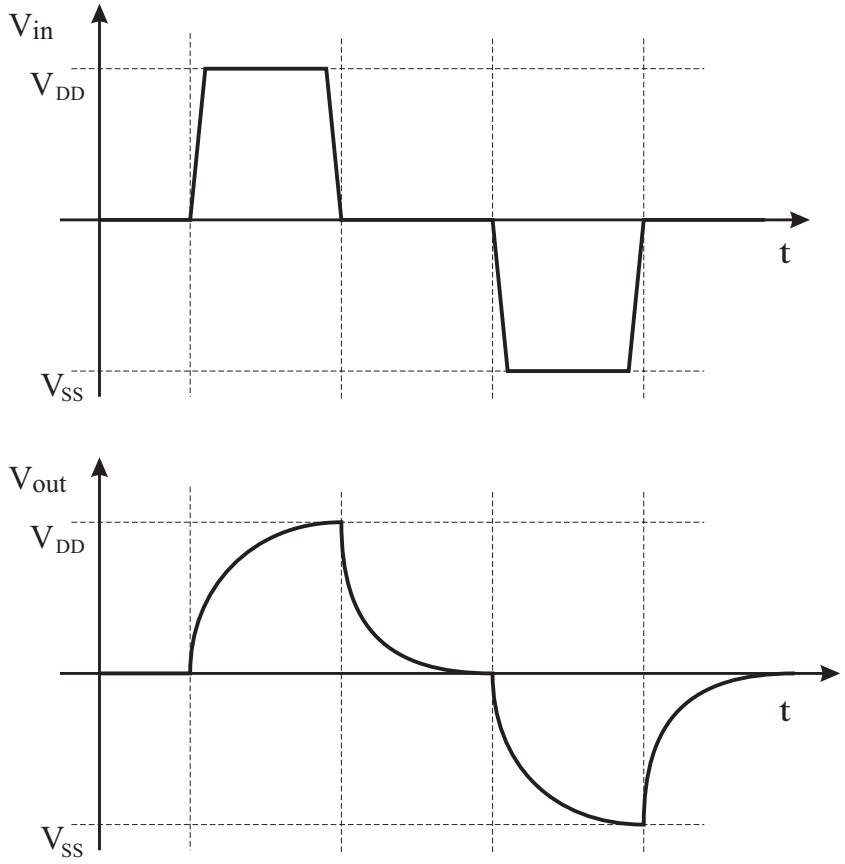


Fig. 2.11 Transient characteristics of a switch composed of CMOS transistors.

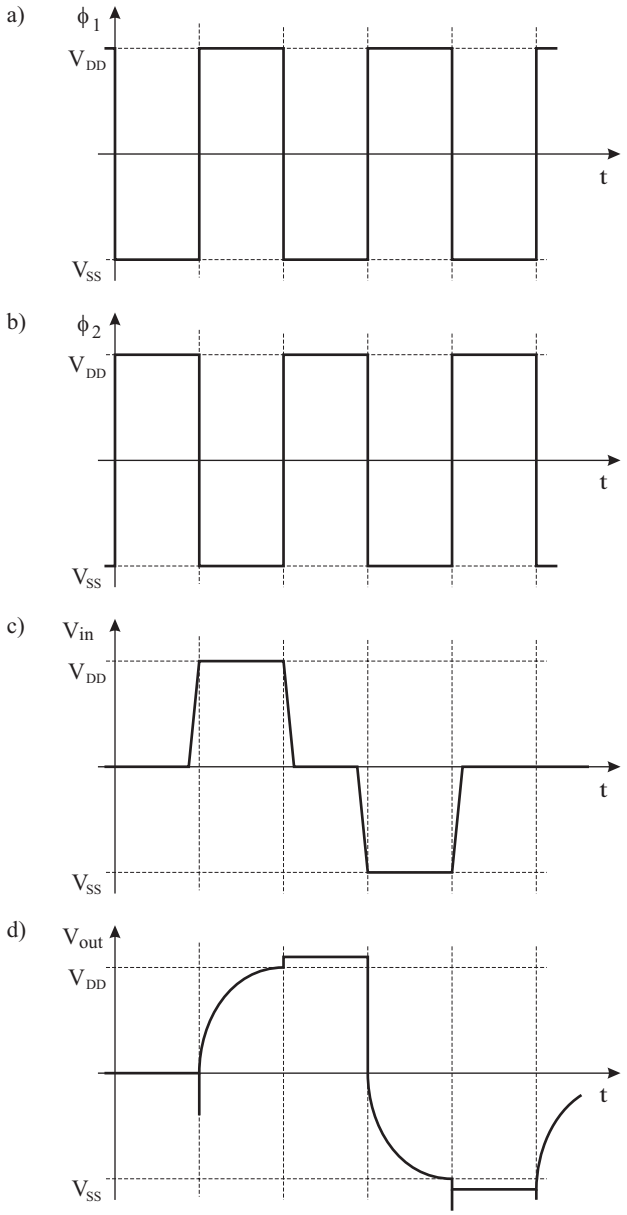
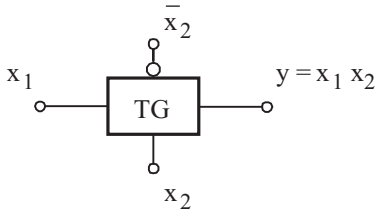


Fig. 2.12 Parasitic effects in a switch composed of MOS transistors.



x_1	x_2	y
0	0	0
1	0	0
0	1	0
1	1	1

Fig. 2.13 Symbol and truth table of a transmission gate composed of a CMOS switch.

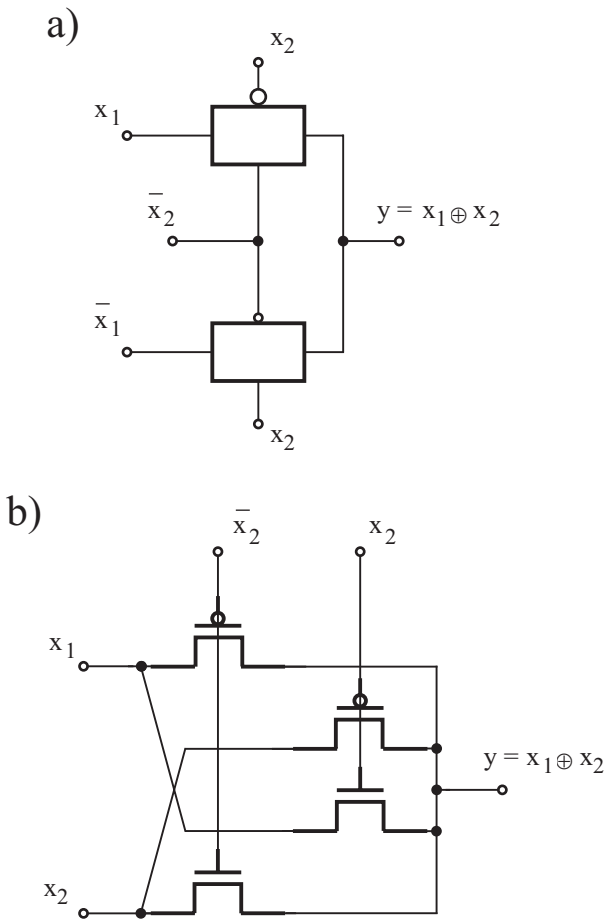


Fig. 2.14 XOR gate based on a transmission gate (a) and on a split-array (b).

signal can be memorized on the output parasitic capacitance. However, in real circuits the leakage currents connect the output node to the ground and $y = 0$. Hence, the transmission gate realizes the AND logic function of the input variables x_1 and x_2.

The realization of the XOR function

$$y = F(x_1, x_2) = x_1\bar{x_2} + \bar{x_1}x_2 = x_1 \oplus x_2, \tag{2.39}$$

is shown in Fig.2.14a. An equivalent XOR gate in the form of a split array, which is more convenient for layout design, is shown in Fig.2.14b.

2.3.5 Inverter

The circuit shown in Fig.2.15, composed of a complementary pair of MOS transistors, is called an inverter. In order to examine its DC transfer curve we assume that the input voltage changes in the range (V_{SS}, V_{DD}). The DC characteristic of the inverter is presented in Fig.2.16. If $V_{out} = (V_{DD} - V_{SS})/2$ for $V_{in} = 0$, then the inverter is called symmetrical. It is possible to obtain the symmetrical inverter if the fabrication process is polarity-symmetric with

$$V_{Tn} = -V_{Tp}, \tag{2.40}$$

and if the inverter is designed for

$$\beta_n = \beta_p. \tag{2.41}$$

For the voltages given in Fig.2.15 we have

$$V_{GSn} = V_{in} - V_{SS}, \;\; V_{DSn} = V_{out} - V_{SS}, \tag{2.42}$$

for the $nMOS$ transistor and

$$V_{SGp} = V_{DD} - V_{in}, \;\; V_{SDp} = V_{DD} - V_{out}, \tag{2.43}$$

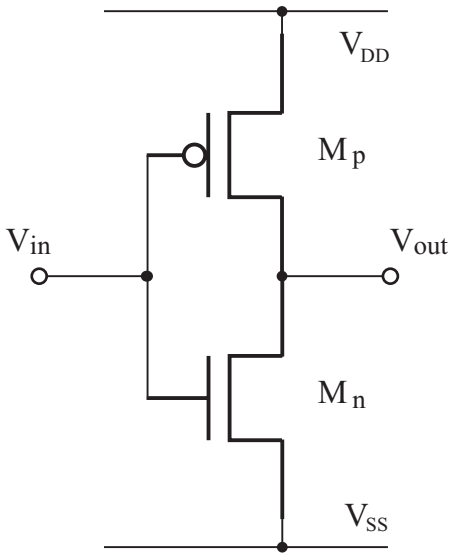


Fig. 2.15 CMOS inverter.

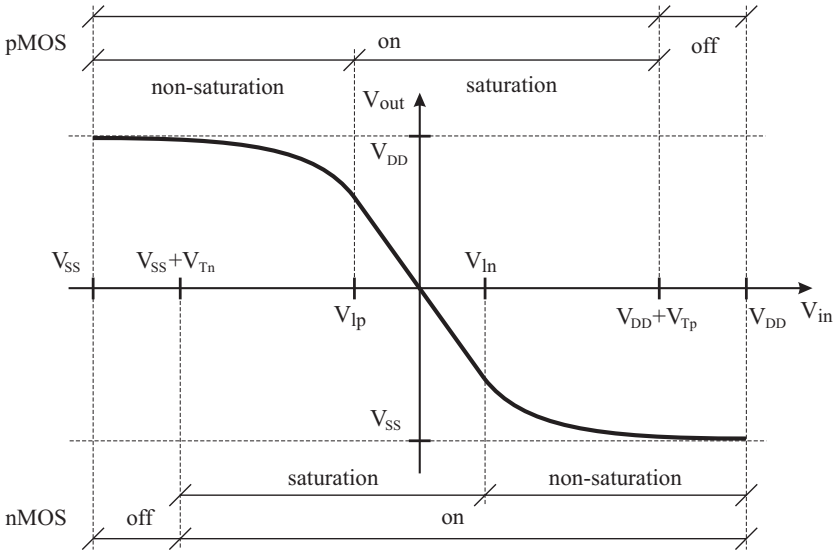


Fig. 2.16 DC transfer curve of an inverter.

for the $pMOS$. In the inverter characteristic, five ranges of voltage V_{in} in the inverter operation are shown. In the first range, the $nMOS$ transistor is *off*, while the $pMOS$ one is conducting in the non-saturated mode. Hence, V_{out} reaches its maximum value V_{DD}. In the second range, the $pMOS$ transistor is in the non-saturated mode until V_{in} achieves a limit value V_{lp}. However, the $nMOS$ transistor is conducting in the saturated mode, which gives a non-linear decrease of the output voltage V_{out}. In the third range, both transistors are conducting in the saturated mode. This range is located between the points V_{lp} and V_{ln}, which can be calculated on the basis of the saturation voltages (2.4) and (2.10). For example, saturation of an $nMOS$ transistor occurs at the point

$$V_{DSn} = V_{DSn,sat}, \tag{2.44}$$

where

$$V_{DSn,sat} = V_{SGn} - V_{Tn} = V_{in} - V_{SS} - V_{Tn}, \tag{2.45}$$

and

$$V_{DSn} = V_{out} - V_{SS} = -\mu V_{in} - V_{SS}. \tag{2.46}$$

The coefficient μ denotes voltage gain in the origin of the coordinate system

$$\mu = \left| \frac{dV_{out}}{dV_{in}} \right|_{V_{in}=0}, \tag{2.47}$$

or

$$V_{out} = -\mu V_{in}. \tag{2.48}$$

Equations (2.44, 2.45, 2.46) yield

$$V_{in} = V_{ln} = \frac{V_{Tn}}{1+\mu}. \tag{2.49}$$

In the fourth and fifth ranges the $nMOS$ and $pMOS$ transistors reverse operation modes compared to the second and first range, respectively.

Concluding, the most important relations describing the five regions of the DC transfer curve are as follows:

1. $V_{in} \in (V_{SS}, V_{SS} + V_{Tn})$: $V_{GSn} < V_{Tn}$, $V_{SDp} = 0 \leq V_{SDp,sat}$,
2. $V_{in} \in (V_{SS} + V_{Tn}, V_{lp})$: $V_{GSn} > V_{Tn}$, $V_{SDp} \leq V_{SDp,sat}$,
3. $V_{in} \in (V_{lp}, V_{ln})$: $V_{DSn} > V_{DSn,sat}$, $V_{SDp} > V_{SDp,sat}$,
4. $V_{in} \in (V_{ln}, V_{DD} + V_{Tp})$: $V_{SGp} > -V_{Tp}$, $V_{DSn} \leq V_{DSn,sat}$,
5. $V_{in} \in (V_{DD} + V_{Tp}, V_{DD})$: $V_{SGp} < -V_{Tn}$, $V_{DSn} = 0 \leq V_{DSn,sat}$.

2.3.5.1 Inverter as a Basic Amplifier In the third range of the DC transfer curve, in which both transistors are saturated, the inverter can be considered as a transconductance amplifier. The output current of the inverter is given by the equation

$$I_{out} = I_{Dp} - I_{Dn} = \frac{\beta_p}{2}(V_{SGp} + V_{Tp})^2 - \frac{\beta_n}{2}(V_{GSn} - V_{Tn})^2. \tag{2.50}$$

Hence, for the gate voltages given by (2.42, 2.43) we obtain

$$\begin{aligned} I_{out} &= (\beta_p - \beta_n)V_{in}^2/2 - [\beta_p(V_{DD} + V_{Tp}) - \beta_n(V_{SS} + V_{Tn})]V_{in} \\ &+ \beta_p(V_{DD} + V_{Tp})^2/2 - \beta_n(V_{SS} + V_{Tn})^2/2. \end{aligned} \tag{2.51}$$

For $\beta_p = \beta_n$ the first component is cancelled and the output current I_{out} depends linearly on the input voltage V_{in}. The third component denoting DC offset of the output current can also be cancelled for a symmetrical inverter $V_{Tp} = V_{Tn}$ and a symmetrical power supply $V_{DD} = -V_{SS}$.

The output voltage depends on the load. If we assume that the amplifier is not loaded, the output voltage is given by

$$V_{out} = I_{out}R_o, \tag{2.52}$$

where R_o is the total drain-to-source resistance. Hence, the low-frequency, small-signal voltage gain is calculated from

$$\mu = -\frac{V_{out}}{V_{in}} = -\frac{I_{out}R_o}{V_{in}} = \frac{(g_n + g_p)V_{in}}{V_{in}(g_{dsn} + g_{dsp})} = \frac{g_n + g_p}{g_{dsn} + g_{dsp}}, \tag{2.53}$$

where g_n, and g_p are trasconductances and g_{dsn}, and g_{dsp} are drain-to-source conductances in small-signal models of $nMOS$ and $pMOS$ transistors, respectively.

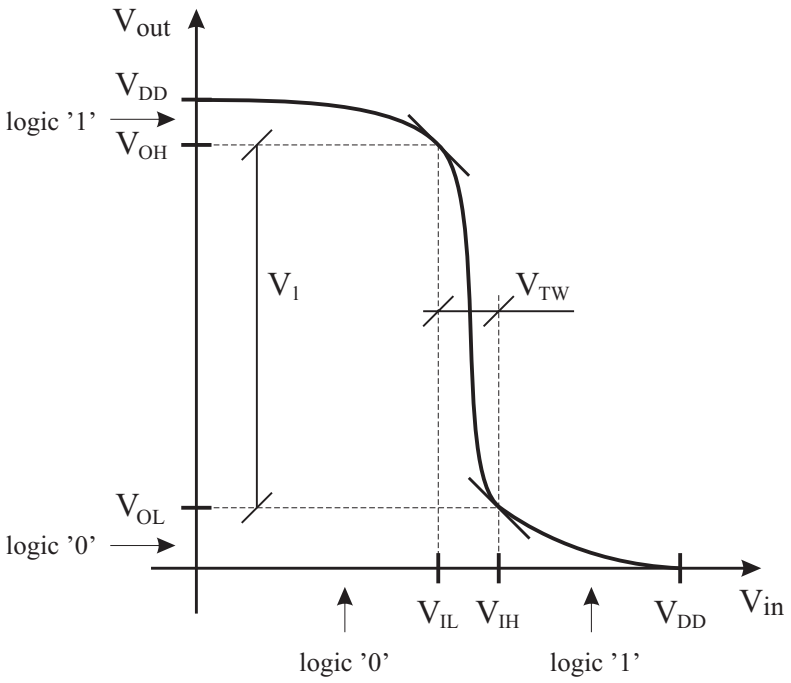
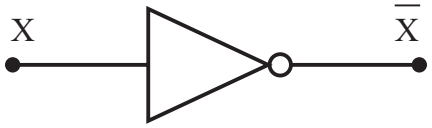


Fig. 2.17 Digital inverter characteristic.



X	$\overline{X}$
0	1
1	0

Fig. 2.18 Symbol and truth table of a CMOS inverter.

2.3.5.2 Inverter as a Digital Logic Circuit On the assumption that $V_{SS} = 0$, the DC transfer curve of the inverter has the form shown in Fig.2.17. Let us associate the logic values "0" and "1" with the voltage ranges in the following way:

$$V_{in} \in < 0, V_{IL} > \doteq \text{"0"}, \quad V_{in} \in < V_{IH}, V_{DD} > \doteq \text{"1"}, \tag{2.54}$$

and

$$V_{out} \in < 0, V_{OL} > \doteq \text{"0"}, \quad V_{out} \in < V_{OH}, V_{DD} > \doteq \text{"1"}. \tag{2.55}$$

The voltages V_{IL}, V_{OH}, and V_{IH}, V_{OL} determine the coordinates of the points where the slope of the digital inverter characteristic is -1, i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1. \tag{2.56}$$

In the regions defined by equations (2.54), (2.55, and (2.56), logic gates work on condition that

$$\left| \frac{dV_{out}}{dV_{in}} \right| < 1, \tag{2.57}$$

and they attenuate the noise added to their input.

We see that for the associations (2.54), and (2.55), the inverter works as a digital element whose symbol and truth table are shown in Fig.2.18.

Apart from V_{IL}, V_{IH}, V_{OL}, and V_{OH} several other voltages are introduced in order to characterize a digital circuit:

1. the logic swing V_l is defined as $V_l = V_{OH} - V_{OL}$ and describes the maximum output voltage variation,

2. the transition width $V_{TW} = V_{IH} - V_{IL}$ is a measure of input sensitivity,
3. the voltage noise margin is introduced both for high and low logic states, as $V_{NML} = V_{IL} - V_{OL}$, $V_{NMH} = V_{OH} - V_{IH}$,
4. the gate threshold voltage V_{th} is defined at the intersection of the inverter characteristic in Fig.2.17 and the unity gain line as the point where $V_{in} = V_{out} = V_{th}$.

The voltages V_l and V_{TW} are shown in Fig.2.17. The voltage noise margins denote the level of voltage separation when digital stages are cascaded. The voltage noise margins must be greater than zero for proper operation of the circuit.

The voltages V_{IL} and V_{IH} can be computed by combining the condition (2.56) with the equation

$$I_{Dn} = I_{Dp}. \tag{2.58}$$

V_{IL} is in the region in which the $nMOS$ transistor is saturated and the $pMOS$ transistor is non-saturated. Hence, I_{Dn} and I_{Dp} are determined by (2.5) and (2.7), respectively, and the equations (2.58), and (2.56) can be written in the form

$$\beta_n(V_{in} - V_{Tn})^2 = \beta_p[2(V_{DD} - V_{in} + V_{Tp}) - (V_{DD} - V_{out})](V_{DD} - V_{out}), \tag{2.59}$$

and

$$\beta_n(V_{in} - V_{Tn}) = \beta_p(V_{DD} - V_{in} + V_{Tp}) - 2\beta_p(V_{DD} - V_{out}). \tag{2.60}$$

From the above equations we obtain $V_{IL} = V_{in}$ by eliminating V_{out}. In the region in which V_{IH} is determined, the $nMOS$ transistor is non-saturated and I_{Dn} is obtained from (2.1) whereas the $pMOS$ transistor is saturated and I_{Dp} is obtained from (2.8). The equations from which $V_{IH} = V_{in}$ can be calculated have the form

$$\beta_n[2(V_{in} - V_{Tn}) - V_{out}]V_{out} = \beta_p(V_{DD} - V_{in} + V_{Tp})^2, \tag{2.61}$$

and

$$2\beta_n V_{out} - \beta_n(V_{in} - V_{Tn}) = -\beta_p V_{DD} + \beta_p(V_{in} - V_{Tp}). \tag{2.62}$$

The definition of the threshold voltage V_{th} given above means that it can be calculated from the relation

$$\beta_n(V_{th} - V_{Tn})^2 = \beta_p(V_{DD} - V_{th} + V_{Tp})^2, \tag{2.63}$$

obtained after equating drain currents of $nMOS$ and $pMOS$ transistors, respectively. Hence, V_{th} obtained from (2.63) has the form

$$V_{th} = \frac{\sqrt{\gamma}V_{Tn} + (V_{DD} + V_{Tp})}{1 + \sqrt{\gamma}}, \tag{2.64}$$

where

$$\gamma = \frac{\beta_n}{\beta_p}. \tag{2.65}$$

The threshold voltage is used to explain the operation of the Schmitt trigger composed of two inverters and shown in Fig.2.19. For the input and output ports denoted in Fig.2.19, the first inverter, composed of transistors Mp_1, and Mn_1, is in the feed-back loop of the second inverter composed of Mp_2 and Mn_2. Suppose that the input voltage V_{in}, applied to the input of the second inverter, is the impulse shown in Fig.2.20a. Because of the feed-back capacitance, composed of gate capacitances of the first inverter transistors, the output impulse is delayed in comparison to the input impulse, as shown in Fig.2.20a. We can observe that the threshold voltage V_{thF} is greater on the rising slope than the threshold voltage V_{thR} on the falling slope. Hence, the trigger has a hysteresis loop, shown in Fig.2.20b, with V_{th} in the forward (F) switching event greater than V_{th} in the reverse (R) one. For steeper slopes, the hysteresis loop is wider.

Another interesting application of inverters is a D flip-flop (DFF), shown in Fig.2.21, controlled by the clock signals Φ and $\bar{\Phi}$ delivered to transmission gates (TG). In the clock phase $\Phi = 0$, the data D from the input is delivered to the input of the first inverter in the data path. In the clock phase $\Phi = 1$, this value is held by the inverter in the feed-back branch of the first loop. In this clock phase, the data $\bar{D}$ is delivered from the output of the first inverter to the input of the second inverter in the data path and held in the same manner as in the first loop. Hence, the data is transferred from the input to the output with the delay equal to one clock period. Using $NAND$ gates instead of inverters in the DFFs allow one to introduce clear and set inputs in these DFFs.

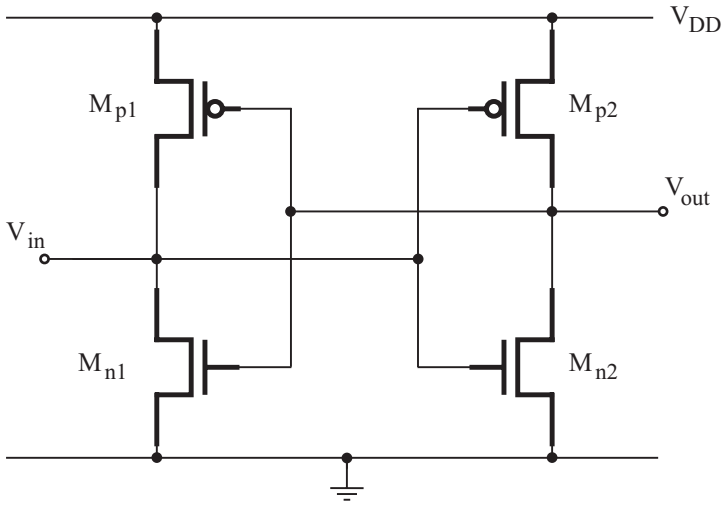


Fig. 2.19 Schmitt trigger composed of two CMOS inverters.

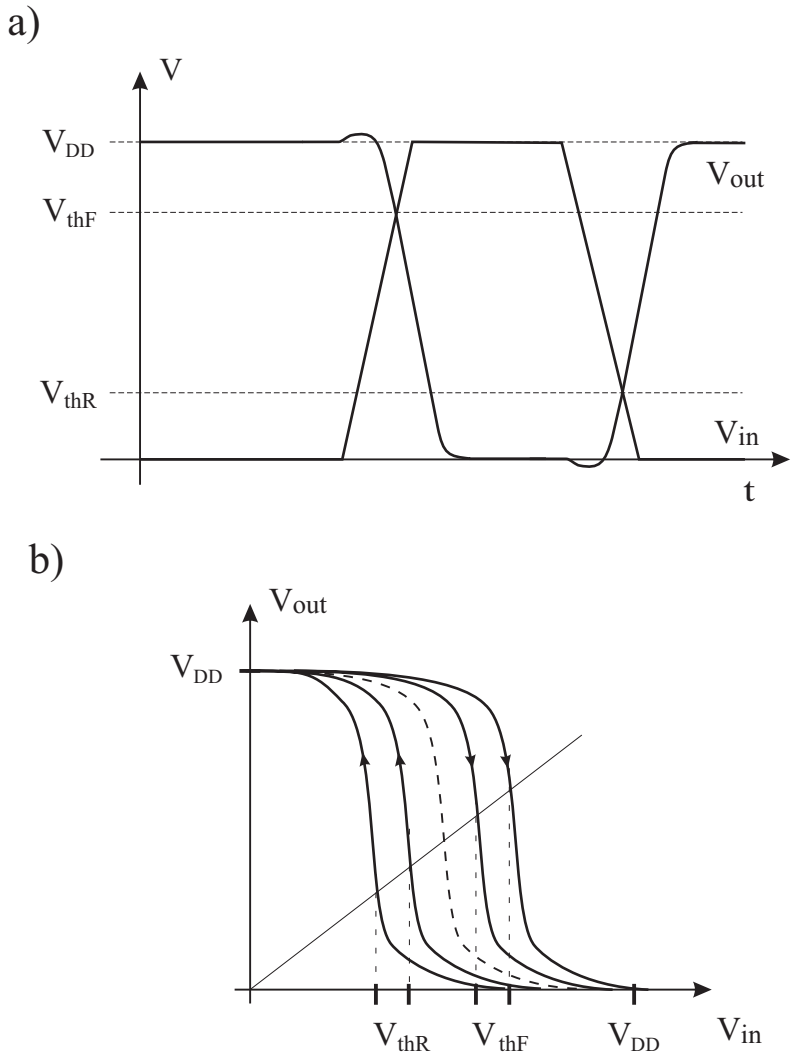


Fig. 2.20 Input and output waveforms (a) and hysteresis (b) of Schmitt trigger.

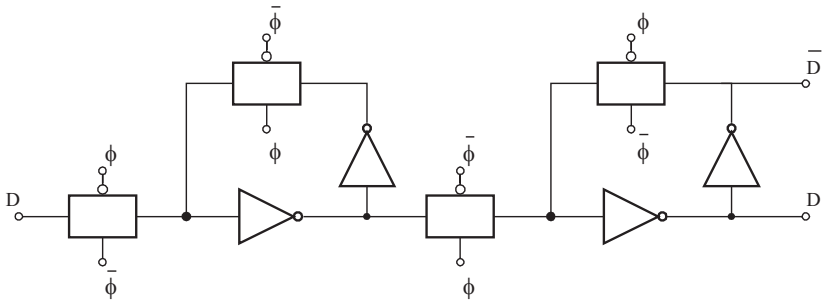


Fig. 2.21 D flip-flop composed of inverters and transmission gates.

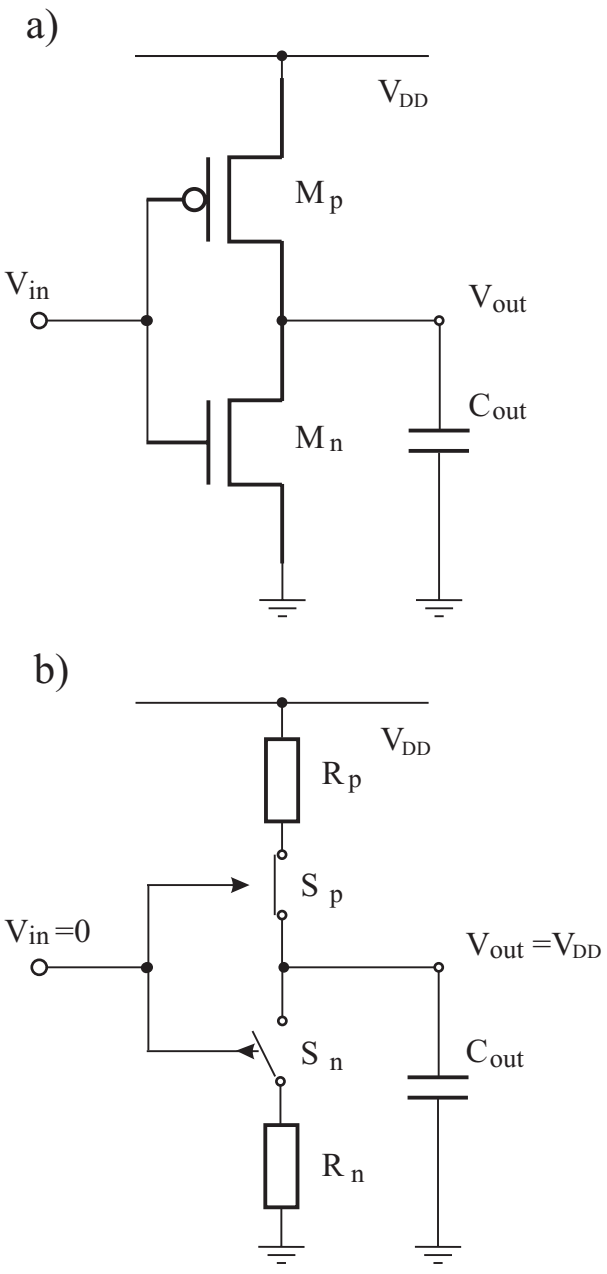


Fig. 2.22 Inverter terminated by capacitance (a) and its transient switch model (b).

Transient characteristics determine the speed of digital circuit operation. Let us consider the inverter terminated with capacitance C_{out}, presented in Fig.2.22. The output capacitance includes several components. The most important components are drain-bulk parasitic capacitances C_{DBn}, and C_{DBp} and gate-drain parasitic capacitances C_{GDn}, and C_{GDp} of the complementary transistors and the capacitance of an interconnection with the next logic stage. The parasitic capacitances of both stages should be taken into account. The simple model of the inverter, which can be used in order to estimate the switching time, is presented in Fig.2.22.b. We see that transistors play the role of switches and, depending on the input signal, C_{out} is charged through R_p or discharged through R_n. It follows from the considerations presented in the section concerning switches that the formulas (2.17) and (2.19) can be used to calculate these resistances, with the gate-source voltages equal to V_{DD}. Hence, the discharge time constant is given by

$$\tau_n = R_n C_{out}, \tag{2.66}$$

where

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}, \tag{2.67}$$

and the charge time constant by

$$\tau_p = R_p C_{out}, \tag{2.68}$$

where

$$R_p = \frac{1}{\beta_p(V_{DD} + V_{Tp})}. \tag{2.69}$$

From these formulas, for desired time constants we get the following aspect ratios W/L of the transistors:

$$\left(\frac{W}{L}\right)_n = \frac{C_{out}}{k'_n \tau_n (V_{DD} - V_{Tn})}, \tag{2.70}$$

and

$$\left(\frac{W}{L}\right)_p = \frac{C_{out}}{k'_p \tau_p (V_{DD} + V_{Tp})}. \tag{2.71}$$

Assuming that the high-to-low time is estimated by $t_{HL} \approx 3\tau_n$ and the low-to-high time by $t_{LH} \approx 3\tau_p$, we define the maximum switching frequency as

$$f_{max} = \frac{1}{t_{HL} + t_{LH}}. \tag{2.72}$$

Let us note that real logic gates are usually much slower in comparison with an estimation given by (2.72).

2.3.6 Current Mirror

A simple realization of a current mirror composed of two $nMOS$ transistors is presented in Fig.2.23. The transistor $M0$ is in diode connection, whereas the gate of the transistor $M1$ is connected with the gate of $M0$ and $V_{GS0} = V_{GS1} = V_{GS}$. The coefficient α_1 is determined by aspect ratios of both transistors

$$\alpha_1 = \frac{W_1/L_1}{W_0/L_0}. \tag{2.73}$$

Assuming that the bias current I_B keeps both transistors in a saturated mode, we have

$$\frac{\alpha_1 I_B - i_{out1}}{I_B + i_{in}} = \frac{\beta_1 (V_{GS} - V_{Tn})^2}{\beta_0 (V_{GS} - V_{Tn})^2}, \tag{2.74}$$

or

$$\frac{\alpha_1 I_B - i_{out1}}{I_B + i_{in}} = \frac{W_1/L_1}{W_0/L_0} = \alpha_1, \tag{2.75}$$

and

$$i_{out1} = -\alpha_1 i_{in}. \tag{2.76}$$

If $\alpha_1 = 1$ then the circuit mirrors the input current at its output.

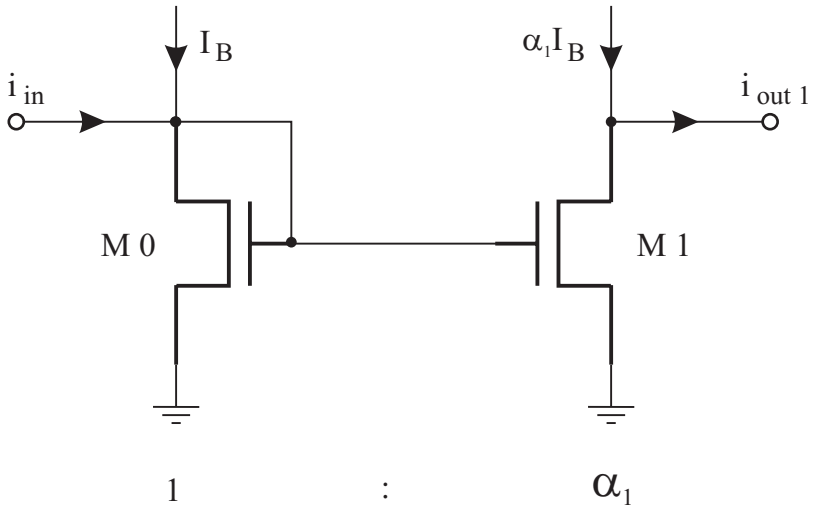


Fig. 2.23 Current mirror.

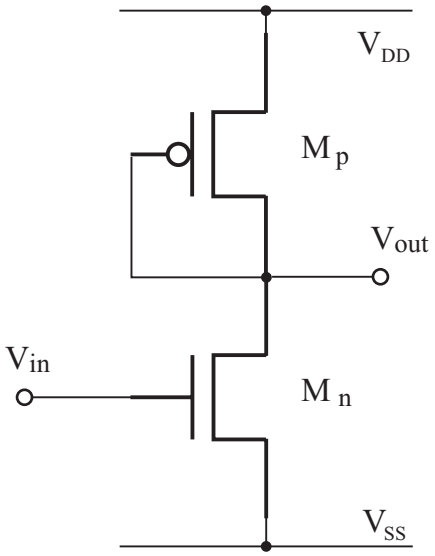


Fig. 2.24 Amplifier stage.

Current mirrors with multiple outputs can be obtained by adding transistors $M2 \ldots Mn$ connected to $M0$ in the same manner as $M1$ and described by the coefficients

$$\alpha_i = \frac{W_i/L_i}{W_0/L_0}, \quad i = 2, \ldots, n. \tag{2.77}$$

In this case we have

$$i_{outk} = -\alpha_k i_{in} \quad , k = 2, \ldots, n. \tag{2.78}$$

2.3.7 Amplifier Stage

An amplifier stage composed of a pair of $nMOS$ and $pMOS$ transistors is shown in Fig.2.24. The $pMOS$ transistor is diode connected. The circuit in which the gate of the $pMOS$ transistor is connected to the reference voltage source V_B is also often used. In the circuit shown in Fig.2.24, the $pMOS$ transistor is in the saturated mode. If

$$V_{out} > V_{in} - V_{Tn}, \tag{2.79}$$

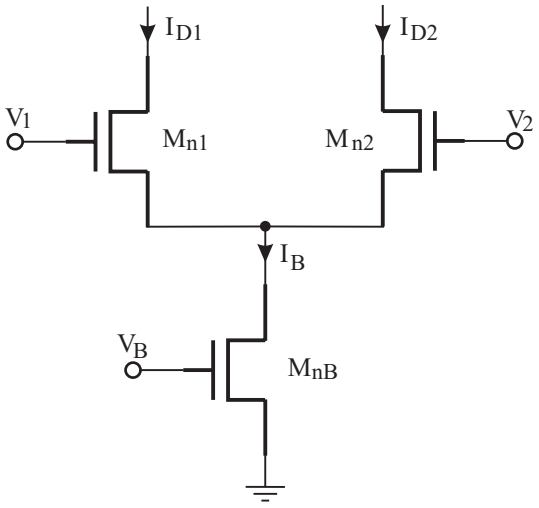


Fig. 2.25 Differential stage.

the $nMOS$ transistor is in the saturated mode, too. Hence, equating the drain currents of both transistors gives

$$\frac{\beta_p}{2}(V_{DD} - V_{out} + V_{Tp})^2 = \frac{\beta_n}{2}(V_{in} - V_{SS} - V_{Tn})^2, \tag{2.80}$$

and

$$V_{out} = -\sqrt{\frac{\beta_n}{\beta_p}}V_{in} + [\sqrt{\frac{\beta_n}{\beta_p}}(V_{SS} + V_{Tn}) + V_{DD} + V_{Tp}]. \tag{2.81}$$

The coefficient in the first component of equation (2.81) denotes voltage gain of the stage, whereas the second component denotes voltage DC offset.

2.3.8 Differential Stage

Let us consider the circuit presented in Fig.2.25 and called a differential stage. The transistor MnB in this circuit plays the role of a current source that delivers the bias current I_B. Assuming that the transistors $Mn1$ and $Mn2$ are in the saturated mode and have the same transconductances $\beta_{n1} = \beta_{n2}$, we can express the drain currents as

$$I_{D1} = \frac{\beta_n}{2}(V_{GS1} - V_{Tn})^2, \tag{2.82}$$

and

$$I_{D2} = \frac{\beta_n}{2}(V_{GS2} - V_{Tn})^2. \tag{2.83}$$

Hence, the difference voltage between the inputs which is defined by

$$V_d = V_1 - V_2 = V_{GS1} - V_{GS2}, \tag{2.84}$$

can be written in the form

$$V_d = \sqrt{\frac{2I_{D1}}{\beta_n}} - \sqrt{\frac{2I_{D2}}{\beta_n}}, \tag{2.85}$$

or

$$\frac{\beta_n}{2}V_d^2 = I_{D1} + I_{D2} - 2\sqrt{I_{D1}I_{D2}}. \tag{2.86}$$

From this equation and from

$$I_{D1} + I_{D2} = I_B, \tag{2.87}$$

we can express the drain currents with the use of difference voltage as

$$I_{D1} = \frac{I_B}{2} \pm \frac{1}{2}\sqrt{\beta_n I_B V_d^2 - \frac{\beta_n^2}{4}V_d^4}, \tag{2.88}$$

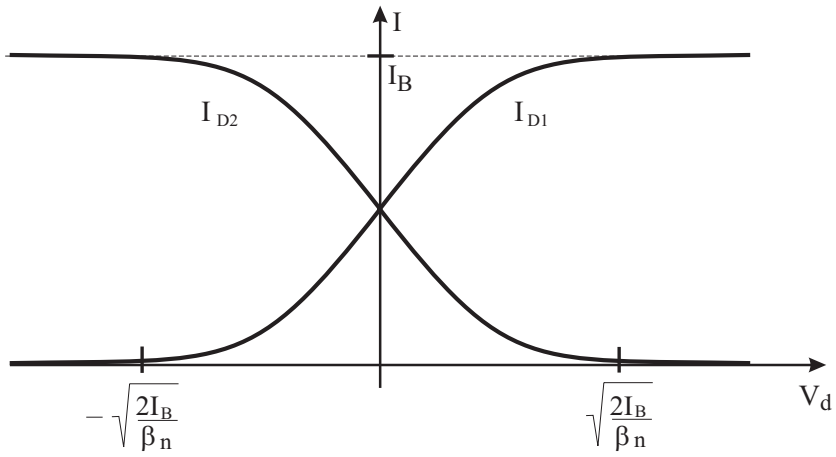


Fig. 2.26 Currents in a differential stage.

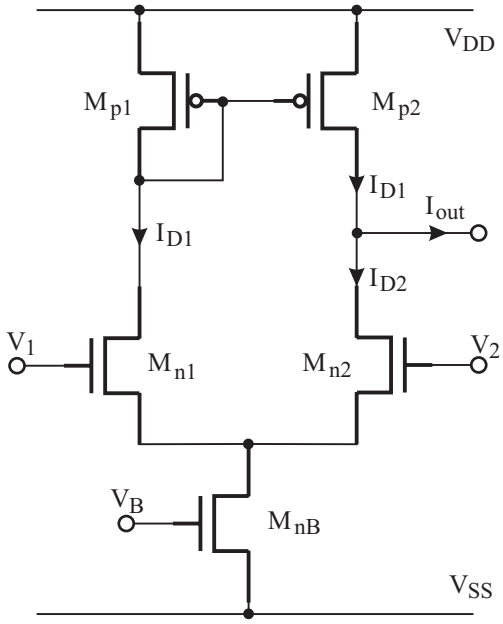


Fig. 2.27 Differential transconductance amplifier.

and

$$I_{D2} = \frac{I_B}{2} \mp \frac{1}{2}\sqrt{\beta_n I_B V_d^2 - \frac{\beta_n^2}{4} V_d^4}. \tag{2.89}$$

The plots of these currents are shown in Fig.2.26.

2.3.9 Differential Transconductance Amplifiers

A circuit composed of a differential stage and a current mirror with *pMOS* transistors, presented in Fig.2.27, has the output current obtained as a difference of drain currents (2.88) and (2.89), in the form

$$I_{out} = I_{D1} - I_{D2} = \sqrt{\beta_n I_B V_d^2 - \frac{\beta_n^2}{4} V_d^4}. \tag{2.90}$$

Assuming that in differential amplifiers

$$\frac{V_d}{2} << \sqrt{\frac{I_B}{\beta_n}}, \tag{2.91}$$

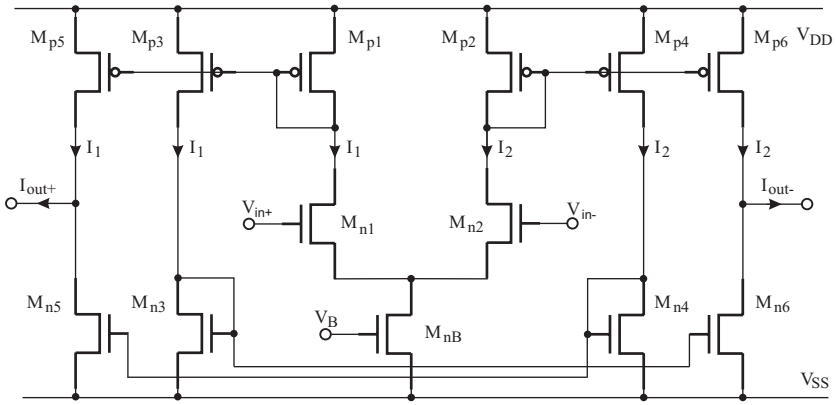


Fig. 2.28 Fully differential transconductance amplifier.

we can now write relation (2.90) in the following way

$$I_{out} = -\sqrt{\beta_n I_B}(V_2 - V_1), \tag{2.92}$$

where

$$g_m = \sqrt{\beta_n I_B}, \tag{2.93}$$

is the differential-mode transconductance of a differential transconductance amplifier. The first input is called the noninverting one whereas the second is the inverting one.

It is possible to realize fully differential trasconductance amplifiers with two outputs, inverting and noninverting (Fig.2.28). Additional current mirrors allow one to obtain two balanced outputs with the output currents given by relations

$$I_{out+} = I_1 - I_2 = \sqrt{\beta_n I_B}(V_{in+} - V_{in-}), \tag{2.94}$$

and

$$I_{out-} = I_2 - I_1 = \sqrt{\beta_n I_B}(V_{in-} - V_{in+}), \tag{2.95}$$

With the use of fully differential amplifiers, switched capacitor circuits in the balanced structure can be obtained. The advantage of switched current and switched capacitor circuits realized in the balanced structure is the cancellation of parasitic effects.

It is worth mentioning here that the transconductance amplifier described by (2.92) can be used as an analog multiplier. On the basis of (2.5), we can rewrite (2.92) in the form

$$I_{out} = -\frac{\beta_n}{\sqrt{2}}(V_B - V_{Tn})(V_2 - V_1). \tag{2.96}$$

Denoting

$$V_B = V_{RF}\ ,\ V_1 = V_{LO}^{+}\ ,\ V_2 = V_{LO}^{-}\ , \tag{2.97}$$

we obtain the transconductor in which output current is proportional to the product of the voltages V_{RF} and V_{LO}. Two of such tranconductors that are connected in the balanced structure compose the Gilbert cell [17]. The Gilbert cell is widely used in digital wireless personal communication systems as so-called mixer. Equations (2.96) and (2.97) show that the mixer is realized as the radio frequency (RF) transconductor in which output current is commutated by the local oscillator (LO).

2.3.10 Operational Amplifiers

The idea of a CMOS operational amplifier (op-amp) is presented in Fig.2.29. The differential stage, composed of $pMOS$ transistors, and a current mirror, composed of $nMOS$ transistors, are components of the first stage of the amplifier. The second stage is composed of a simple voltage amplifier. The compensation feed-back branch contains a capacitor and a resistor in series connection. In Fig.2.29 a MOS transistor implements the resistor.

A macro-model of this operational amplifier is shown in Fig.2.30. Node voltage equations of this circuit can be written in the form:

$$\begin{bmatrix} sC_2 + Y + G_2 & -Y + g_{mn3} \\ -Y & sC_1 + Y + G_1 \end{bmatrix} \cdot \begin{bmatrix} V_{out} \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 \\ -g_{mp1} V_{in} \end{bmatrix}, \tag{2.98}$$

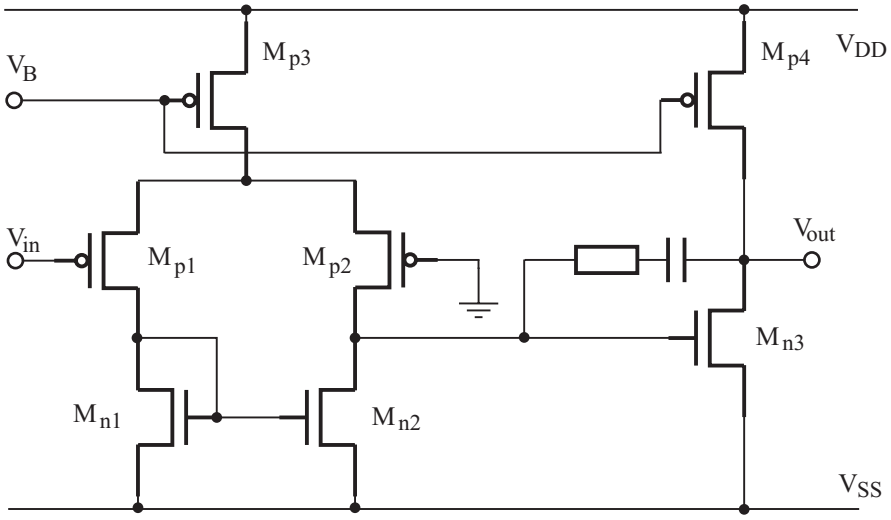


Fig. 2.29 CMOS operational amplifier.

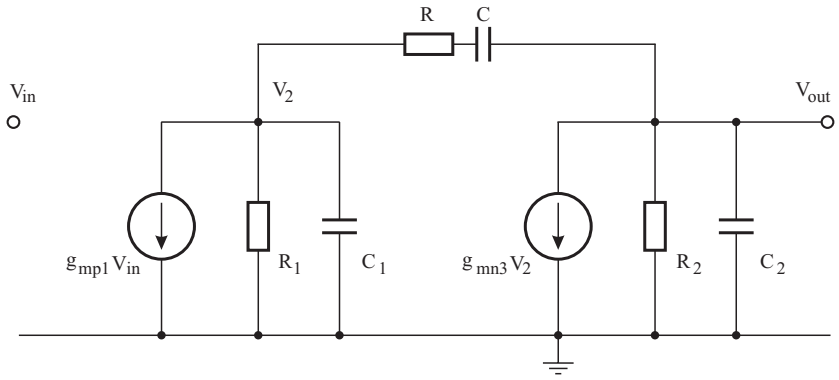


Fig. 2.30 Macro-model of a two-stage operational amplifier.

where Y denotes admittance of the compensation branch and has the form

$$Y = \frac{sC \cdot G}{sC + G} \ . \tag{2.99}$$

From the above equations we obtain the transfer function

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{N(s)}{D(s)} \ , \tag{2.100}$$

where the numerator polynomial

$$N(s) = g_{mp1}(-Y + g_{mn3}) \ , \tag{2.101}$$

and the denominator polynomial

$$D(s) = s^2 C_1 C_2 + s(C_1 + C_2)Y + s(C_1 G_2 + C_2 G_1) + (G_1 + G_2 + g_{mn3})Y + G_1 G_2 \ . \tag{2.102}$$

The numerator and denominator polynomials show that the op-amp has a single zero and two poles. Let us consider the amplifier in which the compensation branch is omitted ($Y = 0$). We have:

$$N(s) = g_{mp1} g_{mn3} \ , \tag{2.103}$$

and

$$D(s) = s^2 C_1 C_2 + s(C_1 G_2 + C_2 G_1) + G_1 G_2 \ . \tag{2.104}$$

The parasitic capacitance C_1 is much smaller than C_2, in which the load capacitance is included. This implies the inequality

$$C_1 G_2 < C_2 G_1 \ . \tag{2.105}$$

For inequality (2.105), the transfer function has complex poles, which are zeros of the polynomial (2.104), and the output waveform of the op-amp is oscillating. In order to obtain

$$C_1 G_2 = C_2 G_1 \ , \tag{2.106}$$

a compensation capacitor with the value approximately equal to the load capacitance can be added in the parallel connection with the capacitance C_1. We have in this case

$$H(s) = \frac{A_o \alpha_p^2}{(s + \alpha_p)^2} \ , \tag{2.107}$$

where

$$\alpha_p = \frac{G_1}{C_1} = \frac{G_2}{C_2} \ , \tag{2.108}$$

is the damping factor and

$$A_o = \frac{g_{mn3} g_{mp1}}{G_1 G_2} \ , \tag{2.109}$$

is the dc gain of the op-amp. The unity-gain frequency ω_1 fulfills the equation

$$\frac{A_o \alpha_p^2}{\omega_1^2 + \alpha_p^2} = 1 \ , \tag{2.110}$$

giving the gain-bandwidth product, $GBP = \omega_1$, in the form:

$$GBP = \sqrt{A_o - 1}\alpha_p \approx \sqrt{A_o}\alpha_p \ . \tag{2.111}$$

This compensation method needs a relatively large additional capacitor that significantly increases the chip area.

In order to explain the role of the compensation branch Y, let us assume first that it contains a capacitor, $Y = sC$, exclusively. Hence, the numerator (2.101) and denominator (2.102) polynomials are as follows:

$$N(s) = g_{mp1}(-sC + g_{mn3}) \ , \tag{2.112}$$

and

$$D(s) = s^2(C_1 C_2 + C_1 C + C_2 C) + s[C_1 G_2 + C_2 G_1 + (G_1 + G_2 + g_{mn3})C] + G_1 G_2 \ . \tag{2.113}$$

On the assumptions that $C \gg C_1$, $C_2 \gg C_1$, $g_{mn3} \gg G_1$, and $g_{mn3} \gg G_2$, the denominator polynomial can be approximated as

$$D(s) \approx s^2 C_2 C + s g_{mn3} C + G_1 G_2 \ . \tag{2.114}$$

This polynomial has two real negative zeros, which are poles of the transfer function. Their values can be estimated when the first and third components in (2.114) are omitted, respectively. Hence, the approximate values of poles are as follows:

$$s'_p = -\alpha'_p \ , \quad s''_p = -\alpha''_p \ , \tag{2.115}$$

where

$$\alpha'_p = \frac{G_1 G_2}{C g_{mn3}} = \frac{g_{mp1}}{A_o C} \ , \quad \alpha''_p = \frac{g_{mn3}}{C_2} \ . \tag{2.116}$$

In order to determine GBP, the numerator polynomial (2.112) and the denominator polynomial (2.114) with omitted third component will be used for the transfer function $H(j\omega)$ approximation. We then have:

$$H(j\omega) = \frac{g_{mp1}(g_{mn3} - j\omega C)}{j\omega C(j\omega C_2 + g_{mn3})} = \frac{1 - j\omega C/g_{mn3}}{j\omega C/g_{mp1}(1 + j\omega C_2/g_{mn3})} \ , \tag{2.117}$$

and the equation $|H(j\omega_1)| = 1$ has the form:

$$1 + (\omega_1 C/g_{mn3})^2 = (\omega_1 C/g_{mp1})^2 [1 + (\omega C_2/g_{mn3})^2] \ . \tag{2.118}$$

Hence, the unity-gain frequency can be estimated by

$$\omega_1^4 \approx \frac{g_{mp1}^2 g_{mn3}^2}{C_2^2 C^2} \ , \tag{2.119}$$

and

$$GBP \approx \sqrt{A_o \alpha'_p \alpha''_p} \ . \tag{2.120}$$

Let us note that in formula (2.116) describing the damping factor α'_p, the capacitance C is multiplied by the amplifier DC gain A_o and the compensation can be realized with the use of a small capacitor. This phenomenon is called the Miller effect. A disadvantage of a Miller compensated amplifier is a right-hand plane zero

$$s_z = \frac{g_{mn3}}{C} \ . \tag{2.121}$$

A resistor is typically used in series connection with C. The value of the resistor allows to cancel the zero. It is even used to put the zero into the left-hand plane.

Aside from GBP, other important parameters that describe the op-amp behavior are: phase margin (PM), slew rate (SR), settling time(t_s), power supply rejection ratio ($PSRR$), and common mode rejection ratio ($CMRR$). These parameters can be expressed in the following way:

1. $PM = 180^o - arg[H(j\omega_1)]$, where ω_1 is the unity-gain frequency,
2. $SR = dV_{out}/dt$, which is the maximum rate of V_{out} change,
3. $t_s = (3 \div 5)\tau$, where the time constant $\tau = 1/\alpha$ is calculated for being the smallest damping factor α,
4. $PSRR = 20 \log \frac{|H_o(j\omega)|}{|H_{supp}(j\omega)|}$, where $H_o(j\omega)$ is an open loop transfer function of an amplifier and $H_{supp}(j\omega)$ is the supply-to-output transfer function,
5. $CMRR = 20 \log \frac{|H_o(j\omega)|}{|H_c(j\omega)|}$, where $H_o(j\omega)$ is an open loop transfer function of an amplifier and $H_c(j\omega)$ is a common-mode transfer function which can be measured for excitation delivered to both inverting and noninverting inputs simultaneously.

Denoting by Q_{ch} the charge delivered to the capacitor C, the above definition of slew-rate can be replaced, on the basis of the relation $Q_{ch} = CV_{out}$, by $SR = I_{ch}/C$, where I_{ch} is the amount of current needed to charge the compensation capacitor C. The settling time t_s, defined as a multiple of the time constant τ, is applicable in linear circuits in which the decrease of voltages is described by the exponential function $v(t) = V_0 \exp(-t/\tau)$. In nonlinear circuits in which voltages can described by other functions, the settling time t_s is defined as a time interval in which the voltage decreases to the level specified as a percentage of its initial value.

2.4 PROBLEMS

1. For the switch presented in Fig.2.7.a, terminated with resistor R, and for the data: $V_{DD} = 1.5V$, $V_{SS} = -1.5V$, $k'_n = 5 \cdot 10^{-5} A/V^2$, $V_{Tn} = 1V$, $W = 10\mu m$, $L = 1\mu m$, $R = 1k\Omega$, $V_{Tn} = 1V$, calculate the maximum value of the output voltage V_{out}. Consider two cases of the pulse applied to the input of the switch:
   (a) the positive pulse with the maximum value V_{DD},
   (b) the negative pulse with the minimum value V_{SS}.
2. Calculate the integral (2.36) of the differential equation (2.32) with the use of substitution (2.34).
3. Assume that V_{in} in Fig.2.9 does not reach a sufficiently big value to introduce the transistor into the saturated mode. Estimate the time constant τ_{ch} in this case. Is the inequality (2.38) still valid under this assumption?
4. Prove that the saturation of a $pMOS$ transistor operating in the inverter occurs at the point given by the formula $V_{lp} = V_{Tp}/(1 + \mu)$.
5. Using equations (2.59), (2.60) and (2.61), (2.62), calculate V_{IL}, V_{IH}, V_{OL}, V_{OH} and V_l, V_{TW}, V_{NML}, V_{NMH} for $V_{DD} = 3V$, $k'_n = 5 \cdot 10^{-5} A/V^2$, $k'_p = 2.5 \cdot 10^{-5} A/V^2$, $V_{Tn} = 1V$, $V_{Tp} = -0.8V$ and $W = 10\mu m$, $L = 1\mu m$ for both kind of transistors.
6. On the basis of relations (2.70), (2.71), calculate the widths of $nMOS$ and $pMOS$ transistors assuming that their length is $L = 2\mu m$ and $V_{DD} = 3V$, $k'_n = 5 \cdot 10^{-5} A/V^2$, $k'_p = 2.5 \cdot 10^{-5} A/V^2$, $V_{Tn} = 1V$, $V_{Tp} = -0.8V$, $\tau_n = 2ns$, $\tau_p = 3.64ns$, $C_{out} = 1pF$. Determine the maximum switching frequency f_{max}?
7. Find the relations (2.88), (2.89), describing the drain currents of a differential stage, as the solution of equations (2.86), (2.87).
8. Calculate the poles and the zero of the transfer function (2.100) for $R = 0$ and the zero for $R \neq 0$.

3

Digital Techniques

Digital techniques are described in many excellent books. In this chapter we will describe the digital techniques that are very frequently used in mixed signal integrated circuit design. In particular, we will describe static and dynamic logic gates and, briefly, finite-state machines and memories.

3.1 STATIC LOGIC CIRCUITS

The general structure of a static logic circuit is presented in Fig.3.1. The inverter shown in Fig.2.15 is a special case of a static logic circuit that realizes the logic function $F = x_1$. The blocks of logic functions F and $\bar{F}$ act as mutually exclusive switches, as the $nMOS$ and $pMOS$ transistors in the inverter. In other words, the $nMOS$ and $pMOS$ logic arrays play the role of respective single transistor in the inverter (Fig.2.15). Depending on the logic values of the input variables $x_1, \ldots, x_n$, the logic function F can achieve a logic values 0 or 1. If $F = 1$ ($\bar{F} = 0$) then the $nMOS$ array is conducting, whereas the $pMOS$ array acts as an open circuit. In this case, the output voltage is low and the logic response $y = 0$. If $F = 0$ ($\bar{F} = 1$), then the $nMOS$ array is an open circuit and the $pMOS$ array is a short circuit, resulting in high output voltage and logic response $y = 1$.

3.1.1 NAND and NOR Gates

The inverter is the only logic circuit in which $pMOS$ and $nMOS$ logic arrays are composed of a single transistor each. Logic circuits containing arrays composed of two transistors in a series or parallel connection are shown in Fig.3.2a,b. In the first logic circuit, the $nMOS$ logic array is conducting when both input signals x_1 and x_2 are equal to 1. In the second circuit, the $nMOS$ array is conducting when at least one of input signals is equal to 1. Hence, the first array realizes the *and* ($x_1 x_2$) operation and the second the *or* ($x_1 + x_2$) operation. As a result, we obtain $NAND$ and NOR gates with the output signals

$$y = \overline{x_1 x_2} \quad , y = \overline{x_1 + x_2} \; . \tag{3.1}$$

In order to estimate transient characteristics of $NAND$ and NOR gates we can use the formulae (2.67) and (2.69) for the transistor channel resistances of $nMOS$ and $pMOS$ transistors, respectively. However, logic arrays are now composed of two transistors in a parallel or series connection. Hence, resistances in relations (2.66) and (2.67) must be replaced by the resultant resistances of two transistors. Consistently, the formulae (2.70) and (2.71) should be modified depending on the kind of the connection.

As an example, let us consider the charging process in the $NAND$ gate. Let us assume that both $pMOS$ transistors are identical. The worst-case situation occurs when only one transistor is conducting. In this case we have

$$(\frac{W}{L})_p = \frac{C}{k'_p \tau_p (V_{DD} + V_{Tp})}, \tag{3.2}$$

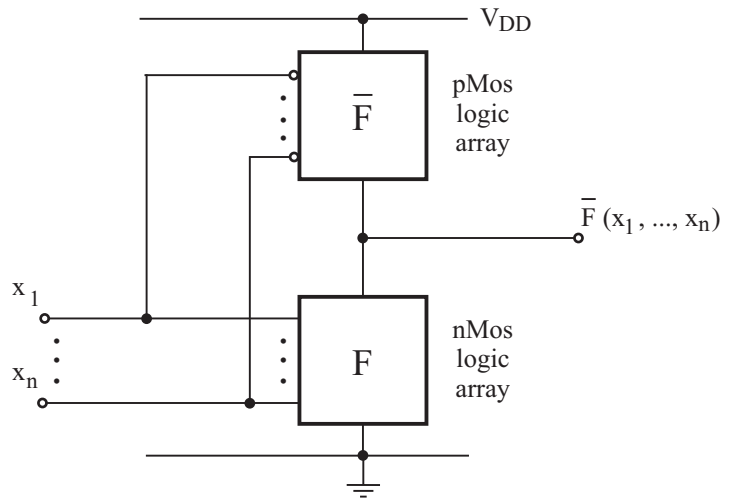
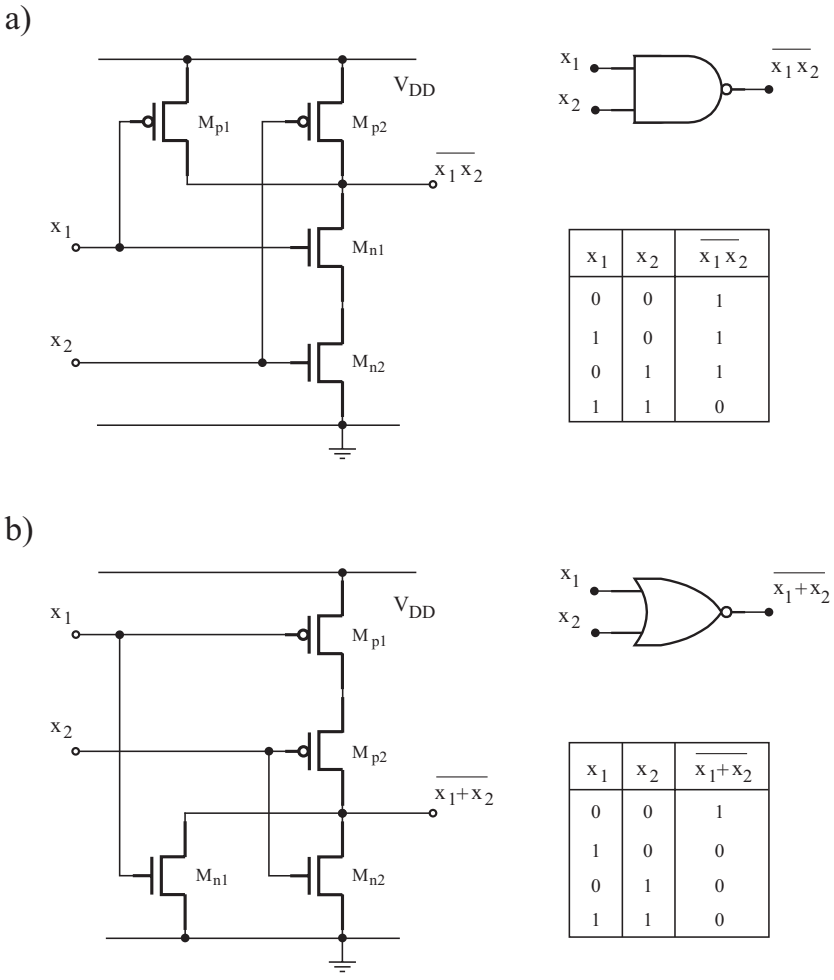


Fig. 3.1 General structure of a static logic circuit.



x_1	x_2	$\overline{x_1 x_2}$
0	0	1
1	0	1
0	1	1
1	1	0

x_1	x_2	$\overline{x_1+x_2}$
0	0	1
1	0	0
0	1	0
1	1	0

Fig. 3.2 NAND (a) and NOR (b) gates with their symbols and truth tables.

where $\tau_p \approx t_{LH}/3$ and t_{LH} is the low-to-high time. Similarly, for the high-to-low response we consider the discharging processes through the series-connected $nMOS$ transistors and we obtain

$$(\frac{W}{L})_n = \frac{2C}{k'_n \tau_n (V_{DD} - V_{Tn})}, \tag{3.3}$$

where $\tau_n \approx t_{HL}/3$ and the factor 2 in the numerator arises as the result of the above-mentioned series connection of the transistors.

For the NOR gate we can obtain the complementary relations

$$(\frac{W}{L})_p = \frac{2C}{k'_p \tau_p (V_{DD} + V_{Tp})}, \tag{3.4}$$

and

$$(\frac{W}{L})_n = \frac{C}{k'_n \tau_n (V_{DD} - V_{Tn})}. \tag{3.5}$$

Since $k'_n > k'_p$, it follows from relations (3.2), (3.3) and (3.4), (3.5) that for the $NAND$ gate $t_{LH} + t_{HL}$ is smaller than for the NOR gate. Hence, the $NAND$ gate that occupies the same chip area as the NOR gate is faster.

The initial values W and L can be calculated on the basis of equations (3.2) and (3.3) for the $NAND$ gate and equations (3.4) and (3.5) for the NOR gate. They can be further improved in an optimization process performed with the use of circuit simulators. The capacitance C includes the input capacitance of the next stage, the capacitance of the connection, and the parasitic capacitances of the gate. It is not determined when the initial values W and L are calculated. Hence, C must be estimated at the beginning and can be specified during the optimization process.

3.1.2 General CMOS Logic Gates

Fig.3.1 presents the general structure of a CMOS static logic gate. The inverter and $NAND$ and NOR gates realize simple logic functions within this general structure. On the basis of these examples, we can formulate rules for implementation of an arbitrary logic function. These rules are as follows:

1. A series connection of $nMOS$ transistors in an $nMOS$ logic array implements the logic multiplication
2. A parallel connection of $nMOS$ transistors implements logic summation
3. Both rules, 1 and 2, also apply if logic blocks are used instead of of single transistors, as shown in Fig.3.3
4. The $pMOS$ logic array is obtained as a complementary circuit to the $nMOS$ array
5. The output of the logic element designed is the complement of the function realized by the $nMOS$ logic array

We shall illustrate these rules by implementing an exclusive-OR (XOR) function, described by the logic function in the form:

$$F = x_1 \oplus x_2 = x_1 \bar{x_2} + \bar{x_1} x_2. \tag{3.6}$$

The symbol and the truth table of an XOR element are shown in Fig.3.4. We see from the truth table that the output of XOR is '0' when $x_1 = x_2$ and '1' when either $x_1 = 1$ or $x_2 = 1$ exclusively. In order to realize the $nMOS$ logic array of XOR, we will use the complement of the function (3.6):

$$G = \bar{F} = (\bar{x_1} + x_2)(x_1 + \bar{x_2}) = \bar{x_1}\bar{x_2} + x_1 x_2. \tag{3.7}$$

The implementation of the XOR element in which the nMOS logic array realizes the function G is shown in Fig.3.5.

A half-adder and a full-adder are important applications of the XOR element. A half-adder calculates the sum s_0 and the carry c_0 of less significant bits (LSB) x_{10} and x_{20} of two n-bit numbers x_1 and x_2 as

$$s_0 = x_{10} \oplus x_{20}, \quad c_0 = x_{10} x_{20}. \tag{3.8}$$

Sum and carry bits of remaining bits x_{1j}, x_{2j}, $j = 1, \ldots, n-1$ are calculated as

$$s_j = x_{1j} \oplus x_{2j} \oplus c_{j-1}, \quad c_j = x_{1j} x_{2j} + x_{1j} c_{j-1} + x_{2j} c_{j-1}, \quad j = 1, \ldots, n-1. \tag{3.9}$$

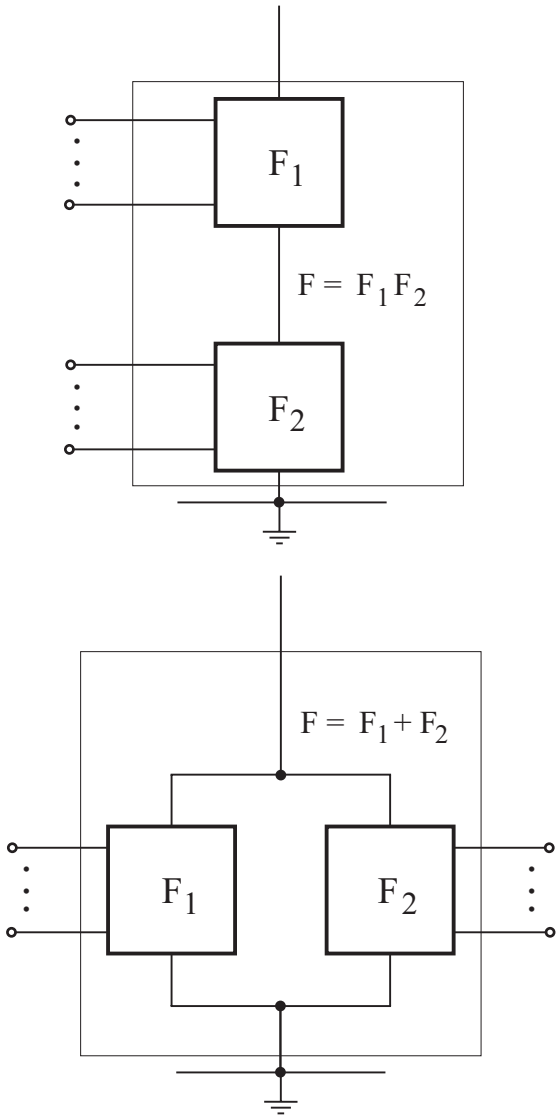
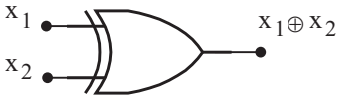


Fig. 3.3 Implementation of the logic functions $F = F_1F_2$ and $F = F_1 + F_2$ by the series and parallel connection of logic blocks.



x_1	x_2	$x_1 \oplus x_2$
0	0	0
1	0	1
0	1	1
1	1	0

Fig. 3.4 Symbol and truth table of an XOR element.

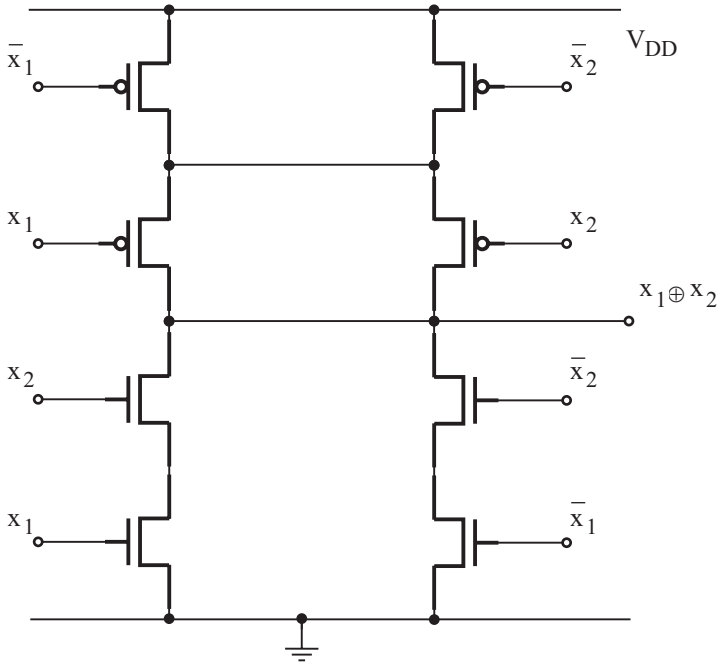


Fig. 3.5 Implementation of an XOR element.

One of possible implementations of the full-adder, shown in Fig.3.6, is obtained after transformation of the logic functions s_j and c_j in (3.9) into the form

$$\begin{aligned} s_j &= (x_{1j} + x_{2j} + c_{j-1})\bar{c_j} + x_{1j}x_{2j}c_{j-1}, \\ c_j &= x_{1j}x_{2j} + c_{j-1}(x_{1j} + x_{2j}), \quad j = 1, \ldots, n-1. \end{aligned} \tag{3.10}$$

3.1.3 Pseudo-nMOS and Pseudo-pMOS Logic

Static $CMOS$ logic gates can be replaced with pseudo-nMOS or pseudo-pMOS devices in order to reduce the number of MOS transistors and, consequently, the chip area and power consumption. Logic gates considered in this section achieve this goal, as they consist of only one logic array, either $nMOS$ or $pMOS$, as shown in Fig.3.7a,b. The second array that appears in $CMOS$ logic gates is now replaced by a single $pMOS$ or $nMOS$ transistor that is the load of the driver array. Let us explain this idea using as an example the pseudo-nMOS inverter presented in Fig.3.8. The $pMOS$ transistor is biased *on*. When the logic value '0' is applied to the input, then the $nMOS$ transistor is *off* and the voltage on the output $V_{OH} = V_{DD}$, which is associated with the logic value '1'. For the input corresponding to '1', both transistors are *on* and the $pMOS$ transistor is saturated, whereas the $nMOS$ one is non-saturated. Hence, for the desired low voltage V_{OL} at the output the following equation for the drain currents

$$\frac{\beta_n}{2}[2(V_{DD} - V_{Tn})V_{OL} - V_{OL}^2] = \frac{\beta_p}{2}(V_{DD} + V_{Tp})^2, \tag{3.11}$$

should be fulfilled. This equation can be written in the form

$$\frac{\beta_n}{\beta_p} = \frac{(V_{DD} + V_{Tp})^2}{2(V_{DD} - V_{Tn})V_{OL} - V_{OL}^2}, \tag{3.12}$$

on the basis of which the transistor channel dimensions can be determined.

Other approaches to digital circuit synthesis implemented in CMOS technology can be found in the literature, e.g. [57]. One approach is the so-called differential cascode voltage switch logic, DCVS, in which two cross-coupled $pMOS$ transistors are introduced as a load. Differential split-level (DSL) can be obtained as the modified DCVS logic.

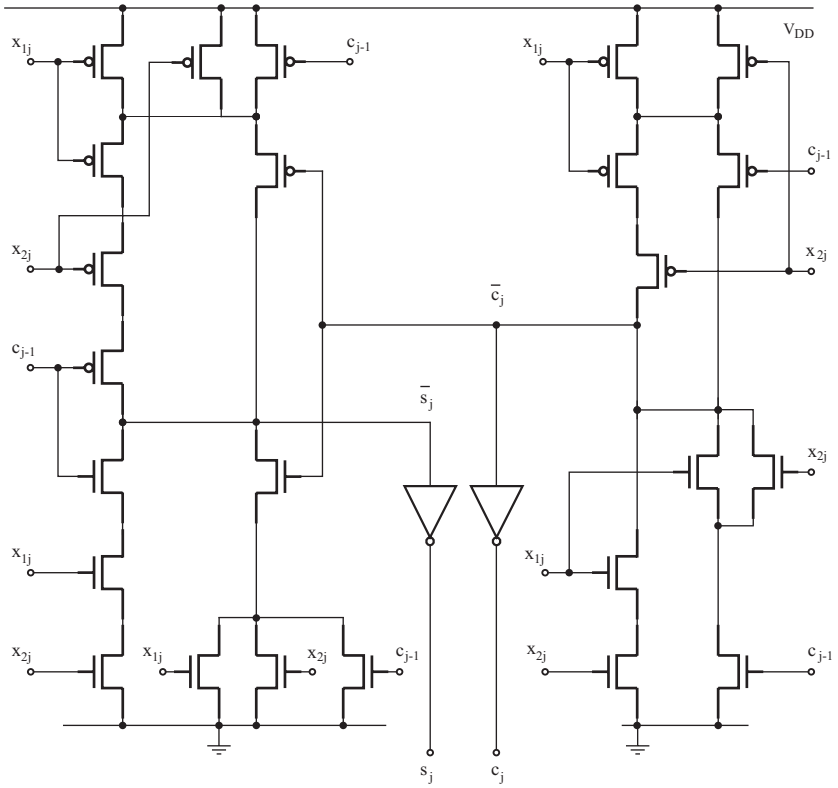


Fig. 3.6 Implementation of a full-adder.

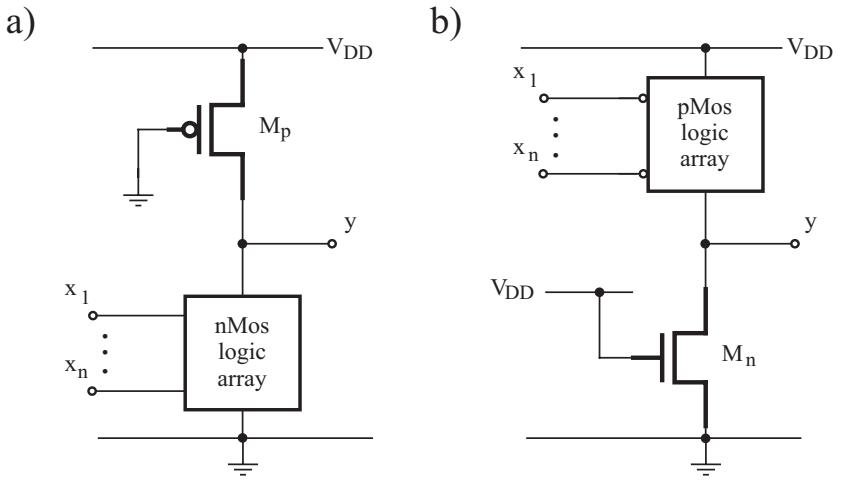


Fig. 3.7 Pseudo-nMOS (a) and pseudo-pMOS (b) gates.

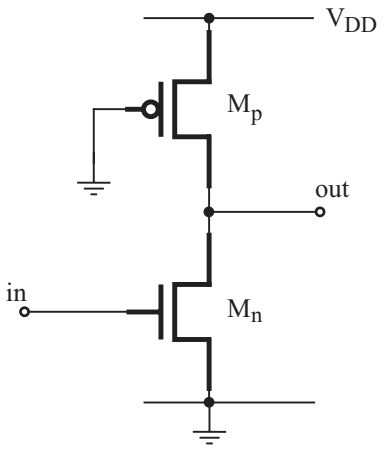


Fig. 3.8 Pseudo-nMOS inverter.

		Q'	
Q	$\bar{S}$	$\Phi = 0$	$\Phi = 1$
0	0	1	1
0	1	0	1
1	0	1	1
1	1	1	0

Table 3.1 Operation of a toggle flip-flop.

3.1.4 Flip-Flops

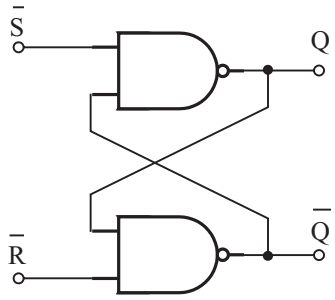
It is possible to construct all types of flip-flops on the basic of the static logic gates introduced above. However, flip-flops based on transmission gates (TG), for example those shown in Fig.2.21, have better performance. Hence, in this section we will consider only two flip-flops based on static logic circuits (two SR flip-flops shown in Fig.3.9 and Fig.3.10). The remaining flip-flops considered here will contain transmission gates.

3.1.4.1 SR Flip-Flops The simplest two-input static logic gates, $NAND$ and NOR, can be used to construct SR flip-flops with the inputs S (set) and R (reset). The $NAND$, based flip-flop is shown in Fig.3.9. The input state $S = R = 1$ is not used because of contradiction at the outputs Q and $\bar{Q}$ which are not complementary for $S = R = 1$. The output is held for $S = R = 0$. Resetting $Q = 0$, and setting $Q = 1$, of the SR flip-flop is achieved for $R = 1$, $S = 0$ and $S = 1$, $R = 0$, respectively.

An SR flip-flop composed of cross-coupled NOR gates is shown in Fig.3.10. In this case, the input state $S = 1$, $R = 1$ is not used. The output state is held for $S = 0$, $R = 0$.

3.1.4.2 Toggle and JK Flip-Flop The DFF shown in Fig.2.21 can be developed with the use of $NAND$ or NOR gates, as shown in Fig.3.11 and Fig.3.12. The first flip-flop, in which two inverters are replaced by $NAND$ gates and the feed-back branch is added, is called a toggle flip-flop (TFF). Let us analyze the operation of the TFF using Table 3.1. The first column in Table 3.1 shows the current state of the TFF. The second column shows the set signal. The last column shows the next state of the TFF in the first ($\Phi = 0$) and second ($\Phi = 1$) half of the clock period. On the basis of Table 3.1, the state diagram shown in Fig.3.11 can be obtained.

The JK flip-flop (JKFF), presented in Fig.3.12, contains two inputs, J and K, introduced with the use of NOR and $NAND$ gates in the feed-back branch. The combinational part of the flip-flop, composed of NOR and $NAND$ gates, is described by the function $D = \overline{J\bar{Q}(K + \bar{Q})} = J\bar{Q} + \bar{K}Q$. The state diagram shown in Fig.3.12 is obtained as a result of the assumption that the next state is equal to the logic value D.



$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$
0	0	x	x
0	1	1	0
1	0	0	1
1	1	Q	$\overline{Q}$

x = not used

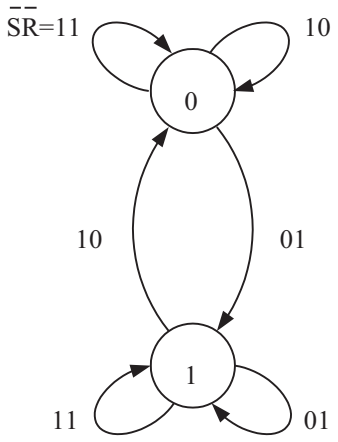
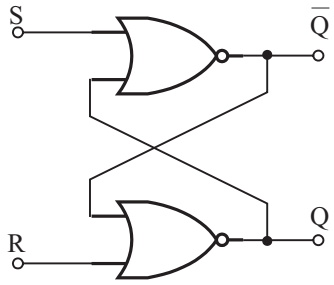


Fig. 3.9 SR flip-flop based on NAND gate.



S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	x	x

x = not used

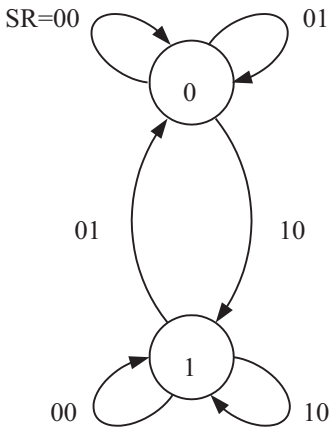


Fig. 3.10 SR flip-flop based on NOR gate.

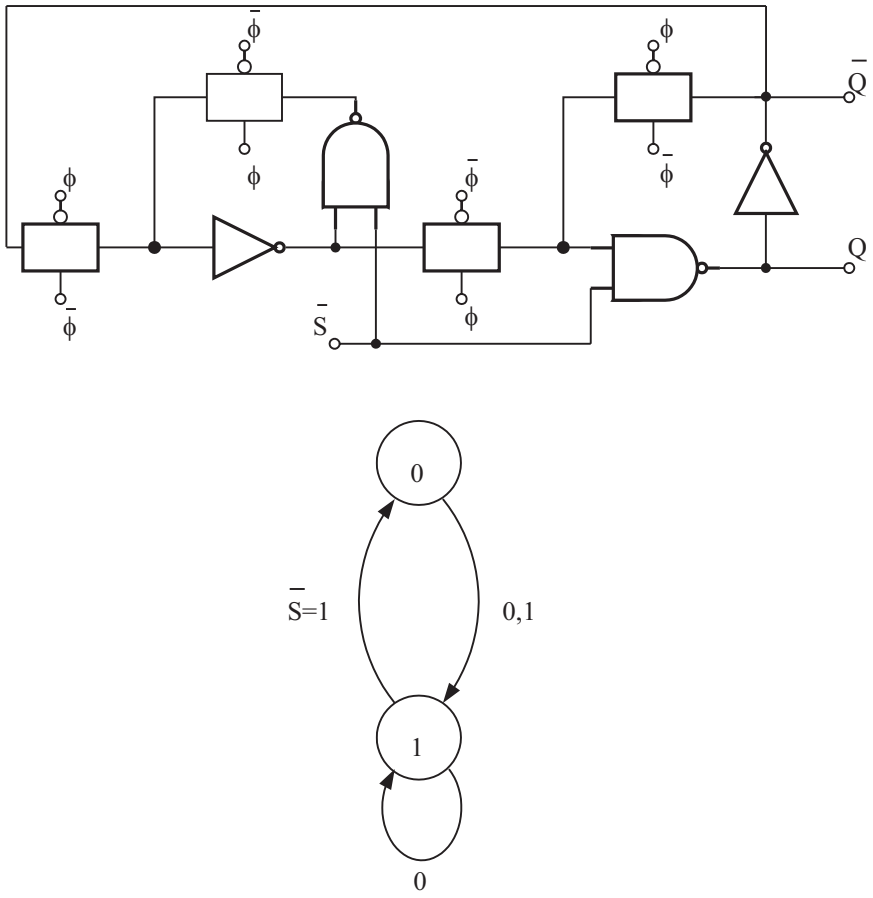


Fig. 3.11 Toggle flip-flop and its state diagram.

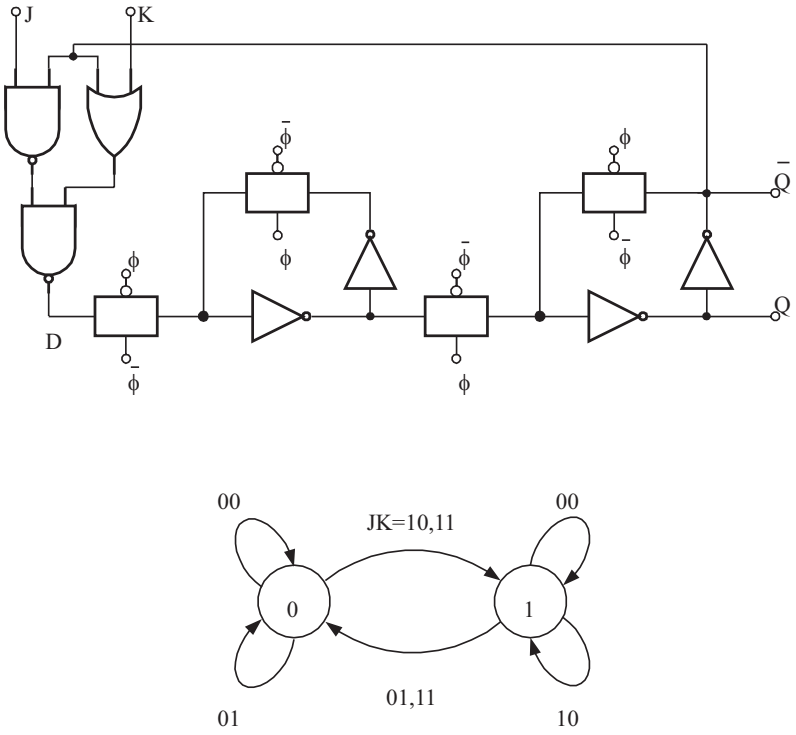


Fig. 3.12 JK flip-flop and its state diagram.

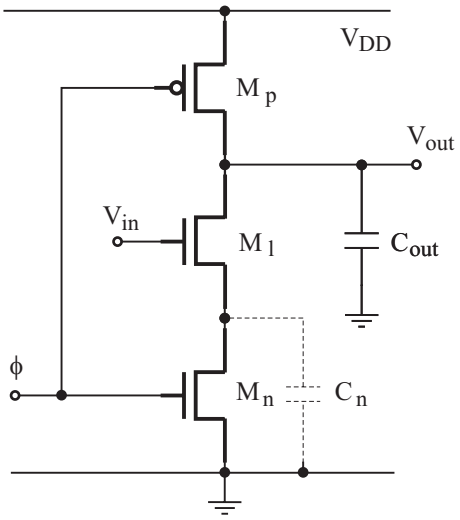


Fig. 3.13 Dynamic nMOS inverter.

3.2 DYNAMIC LOGIC

Dynamic digital circuits are controlled by a two-phase clock, like the flip-flops composed of transmission gates. The kind of logic in which the operation of devices is synchronized by a clock is called synchronous logic.

3.2.1 Dynamic Inverter

The simplest dynamic logic element is the $nMOS$ inverter shown in Fig.3.13. The clock separates the operation of the inverter into two phases: the precharge interval and the evaluate interval. The parasitic capacitors C_{out} and C_n of the corresponding nodes in the circuit in Fig.3.13 are charged or discharged in the precharge and evaluate intervals. The phase $\Phi = 0$, in which the transistor M_p is *on* and the M_n one is *off*, corresponds to the precharge interval. In this phase the capacitor C_{out} is charged to the voltage level $V_{out} = V_{DD}$, regardless of the input signal V_{in}. In the second phase, $\Phi = 1$, the transistor M_p is *off* and the M_n one is *on*, and the operation of the circuit depends on the status of the logic transistor M_l. When the input voltage is low, $V_{in} = V_{IL}$, corresponding to a logic '0', the M_l transistor is *off*, and the output signal is still a logic '1', achieved in the precharge phase. However, for the input signal corresponding to a logic '1', both transistors M_n and M_l conduct and the capacitor C_{out} is discharged. The output is a logic '0'. The maximum clock frequency f_{max} is determined by t_{max}

$$f_{max} = \frac{1}{2t_{max}}, \tag{3.13}$$

where

$$t_{max} = (3 \div 5)max(\tau_{ch}, \tau_{dis}), \tag{3.14}$$

and τ_{ch}, τ_{dis} are charge and discharge time constants. The time constants depend on the design parameters, the width W, and the length L of transistor channels.

The worst case situation in the precharge interval occurs when both capacitors C_{out} and C_n are charged. In order to obtain a simple formula, the resistance R_l of the M_l transistor channel is neglected, and the charge time constant τ_{ch} is described by

$$\tau_{ch} = R_p(C_{out} + C_n), \tag{3.15}$$

where R_p is the M_p transistor channel resistance given by

$$R_p = \frac{1}{\beta_p(V_{DD} + V_{Tp})} = \frac{L}{k'_p W(V_{DD} + V_{Tp})}. \tag{3.16}$$

In the same way, the discharge time constant can be estimated as

$$\tau_{dis} = (R_l + R_n)C_{out}, \tag{3.17}$$

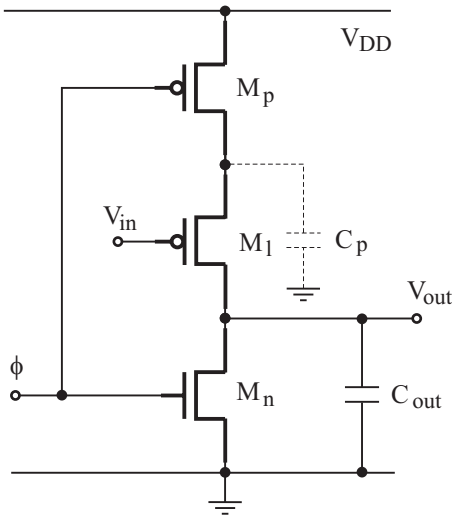


Fig. 3.14 Dynamic pMOS inverter.

and assuming that both transistors M_l and M_n have the same width W and length L of the channels, we obtain

$$\tau_{dis} = \frac{2L}{k'_n W(V_{DD} + V_{Tp})}. \tag{3.18}$$

Time constants τ_{ch} and τ_{dis} can be estimated on the basis of the given maximum clock frequency f_{max}. Formulae (3.17), (3.18) can be used to calculate the initial values of the transistor channel dimensions W and L.

A similar analysis can be performed for a $pMOS$ inverter shown in Fig.3.14.

3.2.2 Dynamic Logic Gates

Dynamic digital gates can be realized with the use of the same $nMOS$ and $pMOS$ logic arrays that are used in static logic circuits. Let us compare $nMOS$ and $pMOS$ inverters in Fig.3.13 and Fig.3.14 with the gates in Fig.3.15 a and b. We see that complex dynamic logic gates are obtained if single M_l transistors are replaced by $nMOS$ and $pMOS$ logic arrays.

Dynamic logic gates can be cascaded in a chain composed of digital gates of alternating type, as shown in Fig.3.16. Let us note that the operation of successive stages in different phases of the clock protects the circuit against logic glitches. The precharge and evaluate intervals occur in opposite phases of the clock for the odd and even stages.

Another system design style that eliminates logic glitches is the domino logic (DL) shown in Fig.3.17, where the stages are buffered by inverters. The output of the previous stage drives the input of the transistor that is the closest to the output of the next stage.

On the basis of the dynamic $nMOS$, $pMOS$ logic, a no-race (NORA) logic can be developed that introduces a cascade connection of the Φ-section and $\bar{\Phi}$-section, terminated by a latch. In order to understand signal races, we will consider a cascade connection of transmission gates (TG) and a logic gate with propagation time t_p (Fig.3.18). It is impossible to generate a clock signal as a perfect square wave. The clock always has finite rise and fall times t_r and t_f. During these transition intervals both transmission gates, TG_1 and TG_2, can partially conduct. Hence, the data bit d_2 delivered during one clock period can reach the output at the moment when the previous data bit d_1 is still there. We can say that d_2 "wins the race" and d_1 is lost. Such possibility does not exist when the gate propagation time is much greater than the rise and fall times ($t_p \gg t_r, t_f$). The effect of signal race also appears when the clock $\bar{\Phi}$ is delayed with respect to Φ by the skew time $t_{skew} \approx t_p$.

As an example of $NORA$ logic application let us consider the full-adder described by the sum and carry logic functions (3.9) and (3.10). The circuit of the adder is shown in Fig.3.19 and its symbol in Fig.3.20. During the $\Phi = 0$ clock interval, the carry logic function is calculated by a dynamic logic gate containing the $pMOS$ array. During the $\Phi = 1$ clock interval, the sum logic function is calculated in the part of the adder containing the $nMOS$ array. In the $\Phi = 1$ phase the latch works as an inverter (the $nMOS$ and $pMOS$ transistors with the gates connected to the clock conduct). In the phase $\Phi = 0$, the latch holds the inverted input logic value at

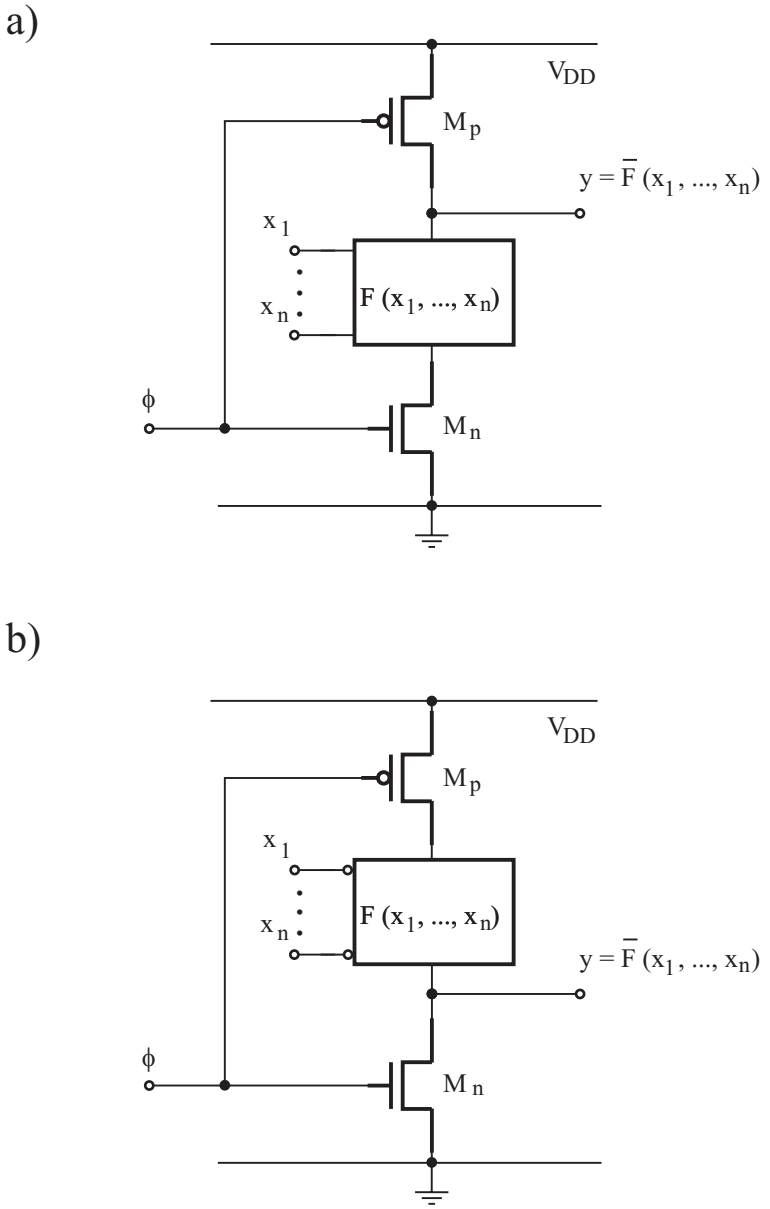


Fig. 3.15 Dynamic logic gates.

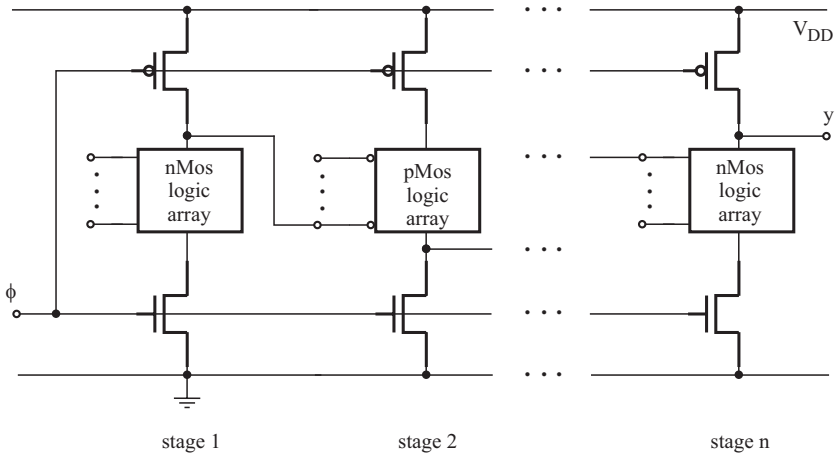


Fig. 3.16 Chain of dynamic logic gates.

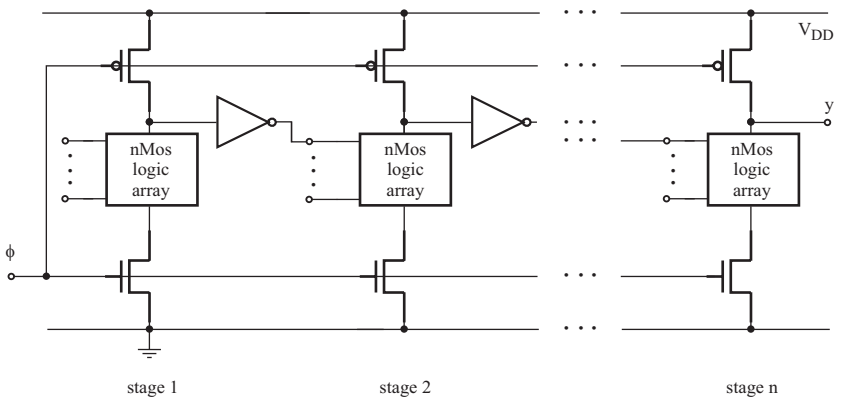


Fig. 3.17 Domino logic chain.

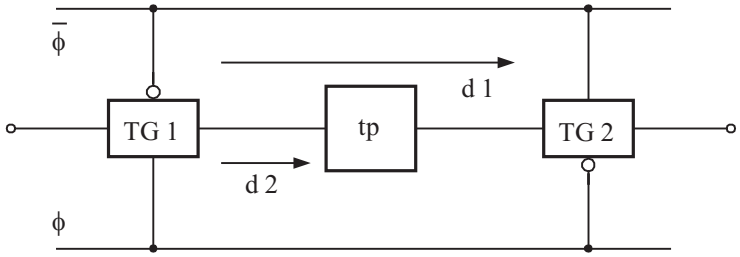


Fig. 3.18 Signal race in a logic circuit.

its output. The delay unit Δ is composed of two latches. The first one has a carry clear input that resets the carry bit before the LSBs x_{10} and x_{20} arrive.

The described adder, which is an example of a pipelined system, can be used for the realization of a serial-parallel multiplier, which calculates the bits p_j of the product of n-bit figures x_1, x_2 in the form

$$p_j = \sum_{k+l=j} x_{1k}x_{2l}, \quad k,l = 0,\ldots n-1, \quad j = 0,\ldots,m, \quad m = 2(n-1). \tag{3.19}$$

The above formula for four-bit words x_1, x_2 can be written in the form

$$\begin{array}{lllll} p_0 = & & & & x_{10}x_{20} \\ p_1 = & & & x_{10}x_{21} & +x_{11}x_{20} \\ p_2 = & & x_{10}x_{22} & +x_{11}x_{21} & +x_{12}x_{20} \\ p_3 = & x_{10}x_{23} & +x_{11}x_{22} & +x_{12}x_{21} & +x_{13}x_{20} \\ p_4 = & x_{11}x_{23} & +x_{12}x_{22} & +x_{13}x_{21} & \\ p_5 = & x_{12}x_{23} & +x_{13}x_{22} & & \\ p_6 = & x_{13}x_{23} & & & \end{array} \tag{3.20}$$

and implemented as the four-bit serial-parallel multiplier shown in Fig.3.21. We see that in this implementation, all bits of x_1 are multiplied by each bit of x_2 and the results are then added with the use of four serial adders to obtain the bits p_j, $j = 0,\ldots,m-1$ of the product.

3.3 FINITE-STATE MACHINES

Flip-flops, introduced in the previous sections, were described with the use of graphs (state-transition diagrams). These graphs contained only two nodes. However, more complex structures are often used to realize controllers of simple processes. Such structures are called finite-state machines, or FSMs. Two examples of three-state machines are shown in Fig.3.22.

The states of a finite-state machine are represented by nodes and input signals, $x_1,\ldots,x_k$, by arcs of the graph, as was in the case of flip-flops. The output signals, $y_1,\ldots,y_l$, are assigned to arcs (for the Mealy

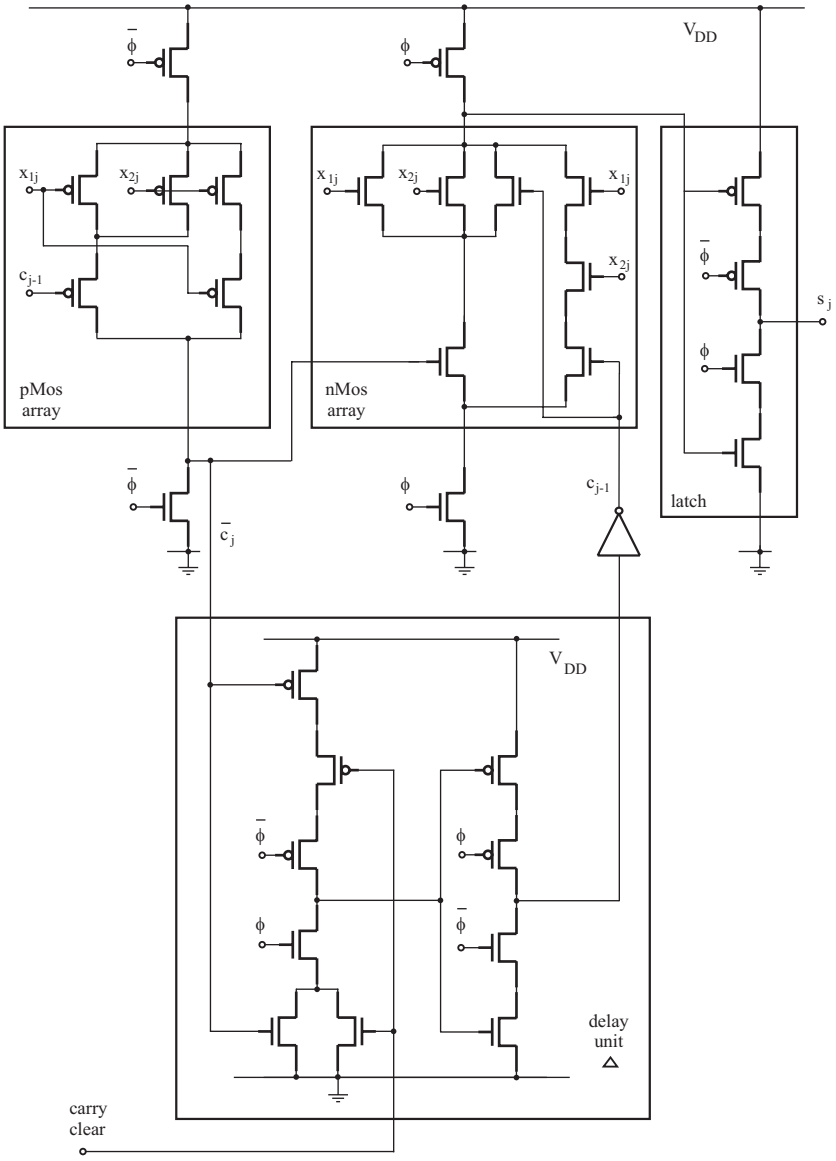


Fig. 3.19 NORA serial full-adder.

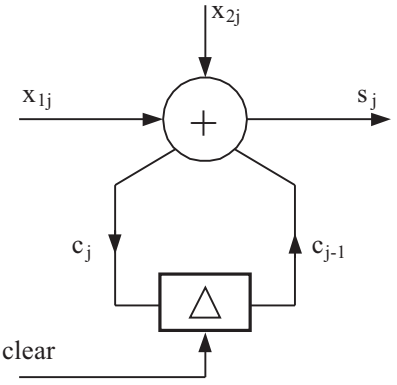


Fig. 3.20 NORA serial full-adder symbol.

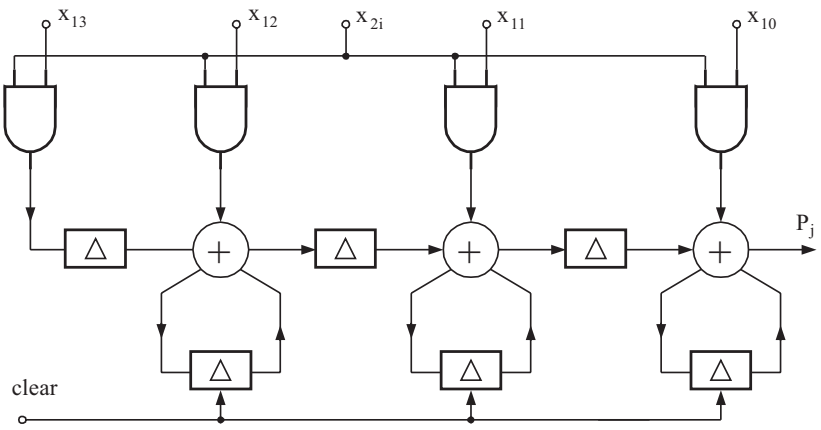
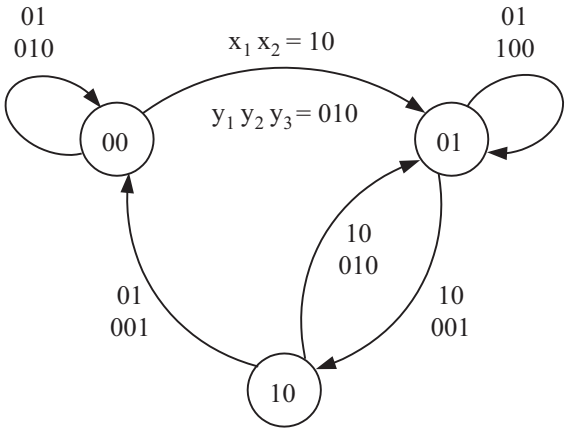


Fig. 3.21 Serial-parallel multiplier.

a)



b)

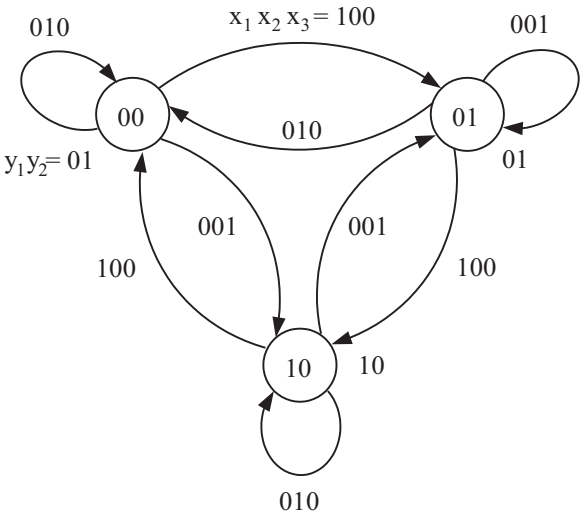


Fig. 3.22 Examples of Mealy (a) and Moore (b) finite-state machines.

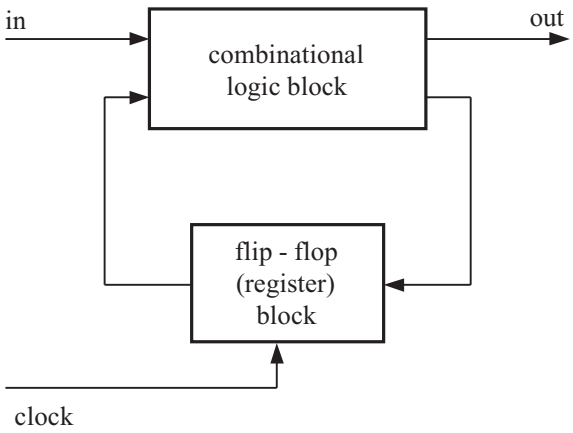


Fig. 3.23 Finite-state machine implemented with the use of a flip-flop block and a combinational logic block.

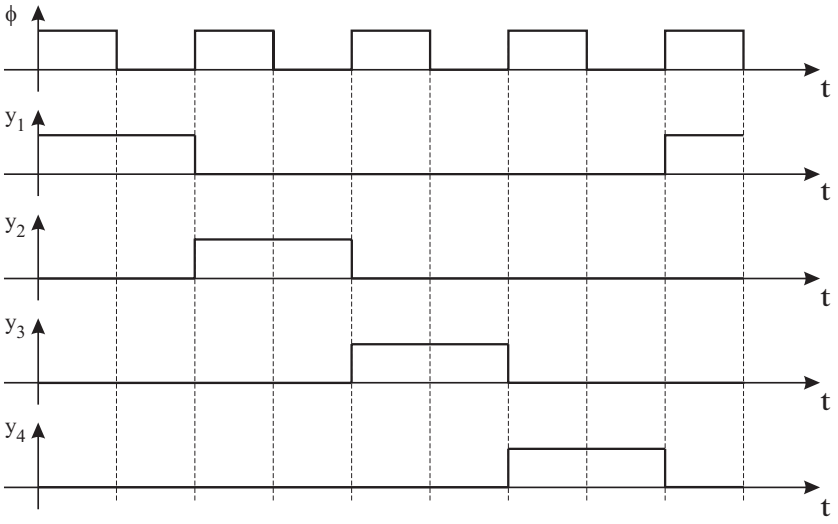


Fig. 3.24 Four-phase clock waveforms.

machine) or to nodes (for the More machine). A finite-state machine can be implemented as the network shown in Fig.3.23. The network consists of a flip-flop block and combinational logic block composed of logic gates.

In order to illustrate the design process of a finite-state machine, let us consider a four-phase clock that generates signals presented in Fig.3.24. Such multiphase clock generators are often used to control circuits implemented in switched capacitor or switched current techniques. The state diagram of the Mealy machine, which is now an autonomous FSM (input signals do not occur and are not assigned to the arcs), is shown in Fig.3.25a.

The design procedure is as follows. Each arc is described in one row of the truth table 3.2. The first column contains bits of the current states, the second one of the next states, and the third one of the outputs. In the general case, when input signals are represented in the FSM, they are included in the first column of the table, too. From this table we obtain the logic equations of the bits of the next states in the form

$$\begin{aligned} Q_1' &= \bar{Q}_1 Q_2 + Q_1 Q_2 = Q_2, \\ Q_2' &= \bar{Q}_1 \bar{Q}_2 + \bar{Q}_1 Q_2 = \bar{Q}_1. \end{aligned} \tag{3.21}$$

These logic equations result in the connections of the DFF shown in Fig.3.25b. The third column of the table implicates the logic equations

$$\begin{aligned} y_1 &= \bar{Q}_1 \bar{Q}_2, \\ y_2 &= \bar{Q}_1 Q_2, \\ y_3 &= Q_1 Q_2, \end{aligned} \tag{3.22}$$

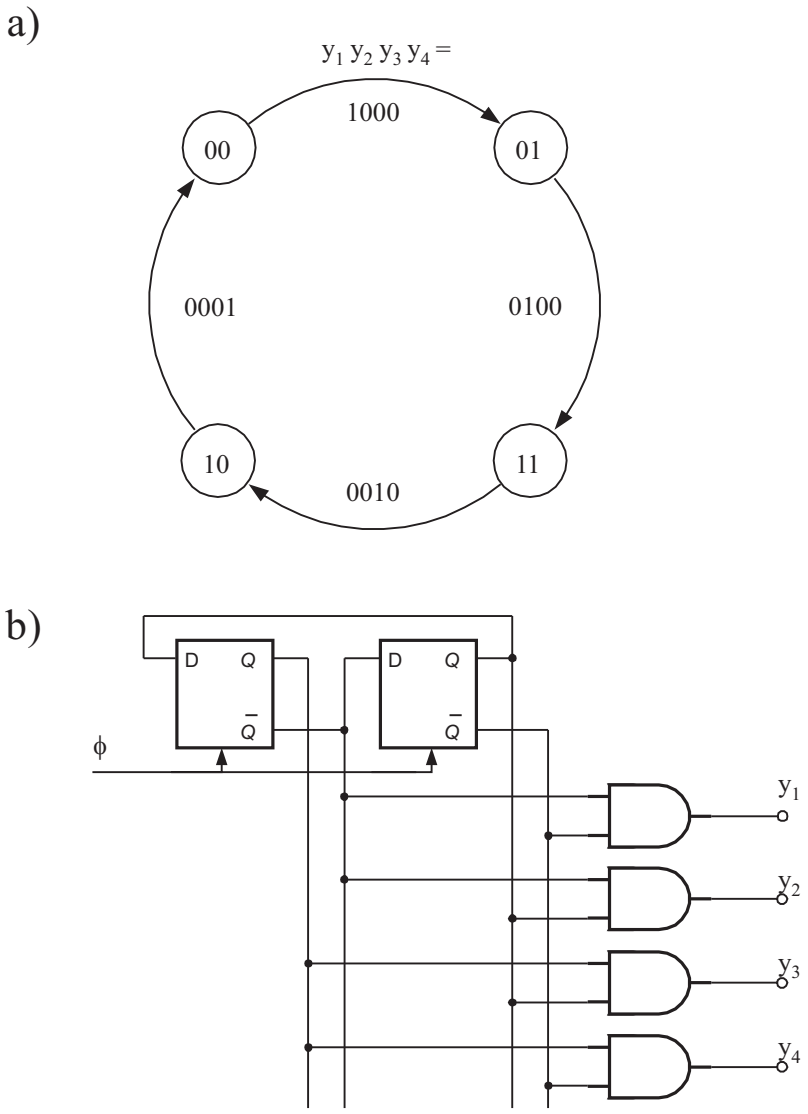


Fig. 3.25 Four-phase clock generator: the state transition diagram (a), and implementation (b).

Q_1	Q_2	Q_1'	Q_2'	y_1	y_2	y_3	y_4
0	0	0	1	1	0	0	0
0	1	1	1	0	1	0	0
1	1	1	0	0	0	1	0
1	0	0	0	0	0	0	1

Table 3.2 State table of a clock generator.

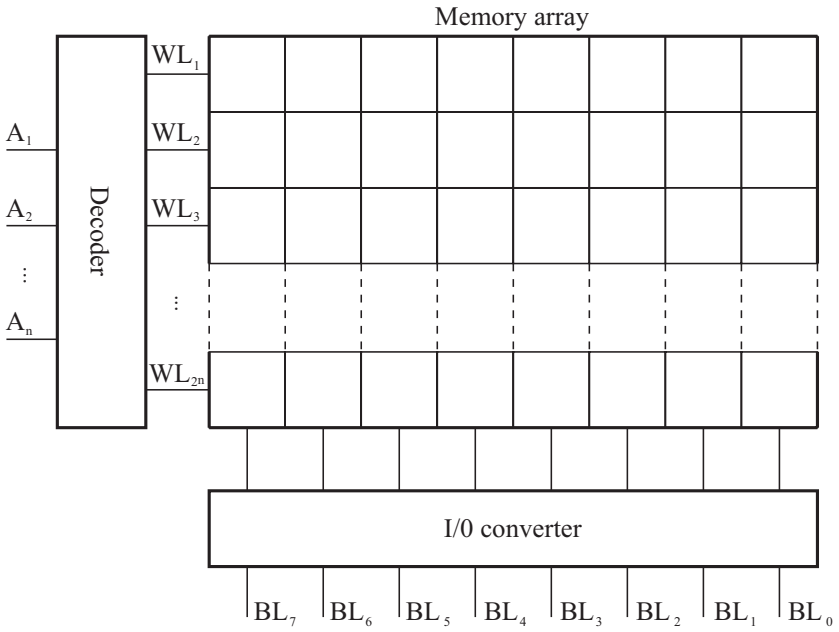


Fig. 3.26 Architecture of a digital memory.

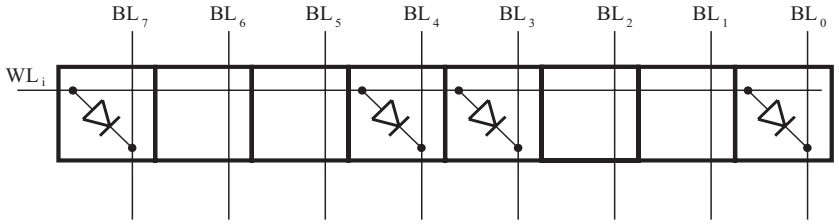


Fig. 3.27 Word implementation of memory based on diodes.

$$y_4 = Q_1\bar{Q}_2,$$

which are implemented with the use of AND gates in the FSM in Fig.3.25b.

3.4 MEMORIES

This section briefly describes digital memories that can be realized in the CMOS technology. A memory can be considered as a matrix of cells (Fig.3.26). Each cell stores one bit of digital data. The memory shown in Fig.3.26 has eight cells in each row of the memory array. The data stored in one row is called a word. The memory shown in Fig.3.26 stores eight-bit (one byte) words. The abbreviation for byte is the capital letter B, hence the word size in our example can be denoted as 8b=1B. Note that *word* is not a synonym of *byte*.

In order to read or write a word from or into the memory, the cells in columns of the memory array are connected to an I/O converter by bit lines (BLs). A set of such wires that together carry a binary number is called a bus. The I/O converter can be composed of resistors or more complicated elements like amplifiers and buffers, depending on the kind of memory. The address delivered to the address bus $A_1, \ldots, A_n$ points at the chosen word of the memory. For this purpose, the decoder, composed of digital gates and multiplexers (Fig.3.26), converts an n-bit address into a logic "1" delivered to one of 2^n word lines (WLs), leaving "0" on the remaining word lines. The memory size depends on the word size as well as on the number of address bus wires. For a 1B word and address bus n=10 we get 1 kB (1024 B) of memory, while for n=16 we get 64 kB of memory.

A simple implementation of a memory word is shown in Fig.3.27. The memory cell contains a diode connecting the word line to the bit line in the case of the bit "1". For the bit "0" of the stored word, the cell is empty. Such a memory implementation contains permanent information that cannot be changed. It is called read-only memory or ROM. A programmable read-only memory (PROM) can be obtained for the memory array completely filled

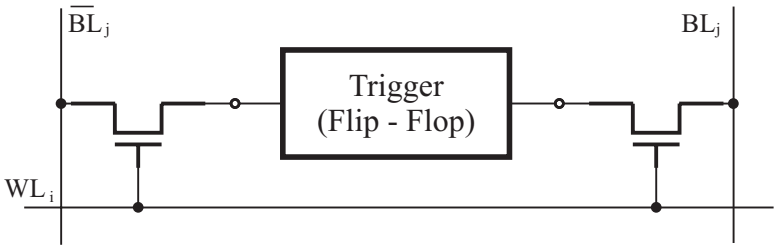


Fig. 3.28 Flip flop memory cell.

with diodes. Selected diodes are disconnected during the programming process. If such connections can be changed and if the programming process can be repeated, then the memory is called erasable programmable read-only memory (EPROM). In this case, the diodes are replaced by MOS transistors that act either as diodes or as open circuits, depending on whether their gates are electrically charged or not. An electrically erasable programmable read only memory (EEPROM) is often called a FLASH memory.

A disadvantage of the read-only memory is that its contents cannot be changed or can be changed by a relatively long programming process. The memory composed of cells that allows fast access both in the read and write modes is called random access memory or RAM. The simplest RAM can be realized with the use of flip-flops introduced as memory cells. Such a cell is shown in Fig.3.28 together with connections to word and bit lines. The Schmitt trigger shown in Fig.2.19 can be put in the cell. A memory that uses triggers to hold bits is called static RAM. Large chip area and high power consumption are disadvantages of static cells. The dynamic RAM cell in which tiny capacitors are used as storage elements is shown in Fig.3.29a. Small stored charges are quickly lost through the connected transistor. Therefore, the dynamic RAM needs a refreshing process before the charge becomes unreadable. Two implementations of the dynamic RAM cell, called Dennard and Kosonocky structures, are shown in Fig.3.29 b and c, respectively. In the Dennard structure, the common plate of capacitors C_0 and C_j is obtained by extension of the source area of the transistor. In this case, the node V is connected to V_{SS}. In the Kosonocky structure, the node V must be connected to the power line V_{DD} in order to obtain the common plate and to realize the junction capacitor C_j.

3.5 PROBLEMS

1. Using static logic circuits, design the complement of the XOR element called exclusive-NOR gate ($XNOR$), realizing the function $F = x_1 \odot x_2 = \overline{x_1 \oplus x_2}$.

2. Using the gate whose general structure is presented in Fig.3.15a, realize a half adder whose sum and carry functions are described by relations (3.8).

3. The state transition diagram in Fig.3.30 describes a two-speed flasher. The flasher emits light only when the output signal L=1. For the button b on (b=1), the oscillations of flashes are twice as fast as for the button b off (b=0). Realize this FSM.

4. Explain why the diode connections in Fig.3.27 cannot be replaced by short circuit connections.

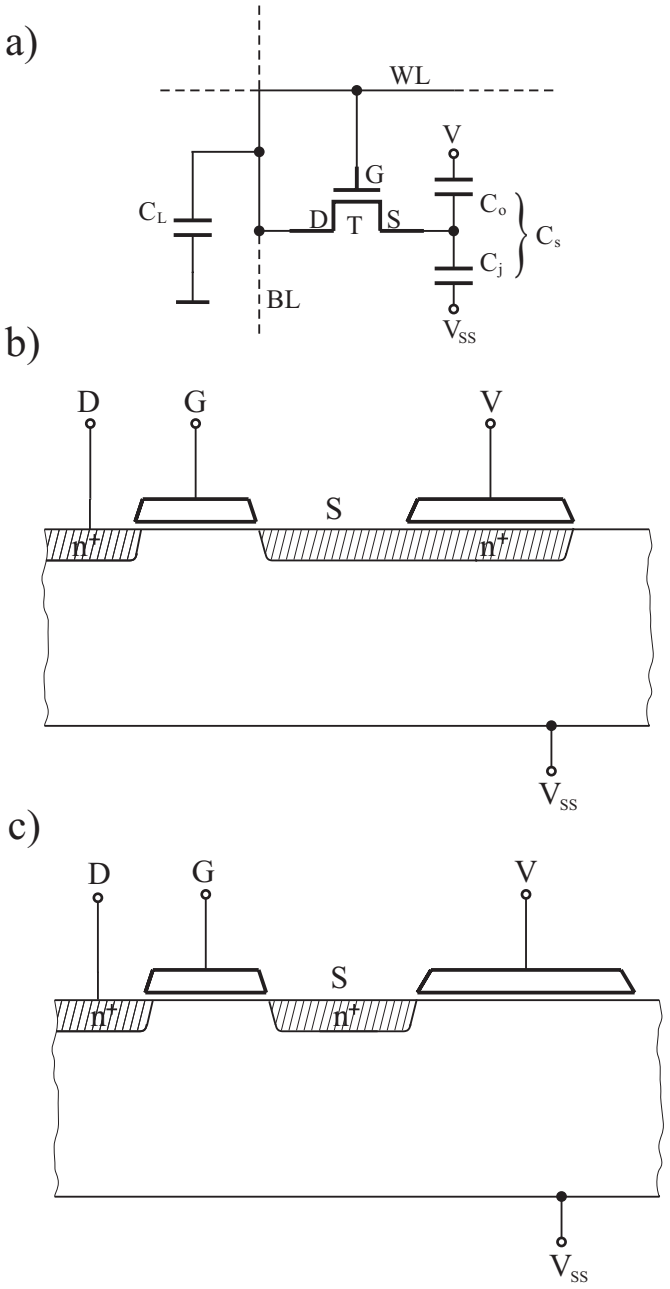


Fig. 3.29 RAM cell composed of a transistor and capacitors: schematic diagram (a) and its implementations in Dennard (b) and Kosonocky (c) structures.

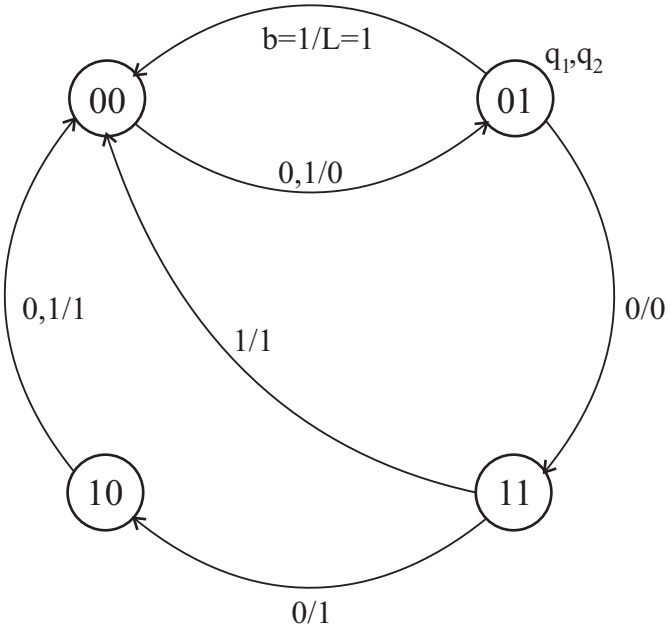


Fig. 3.30 Example of the state transition diagram.

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